# Design challenges of PCIe Gen4 using Altium

*A practical Approach*

DESIGN

FROM CONCEPT
TO MANUFACTURING

WWW.PCBDESIGN.HU

János Lazányi – CEO – PCB Design Kft.

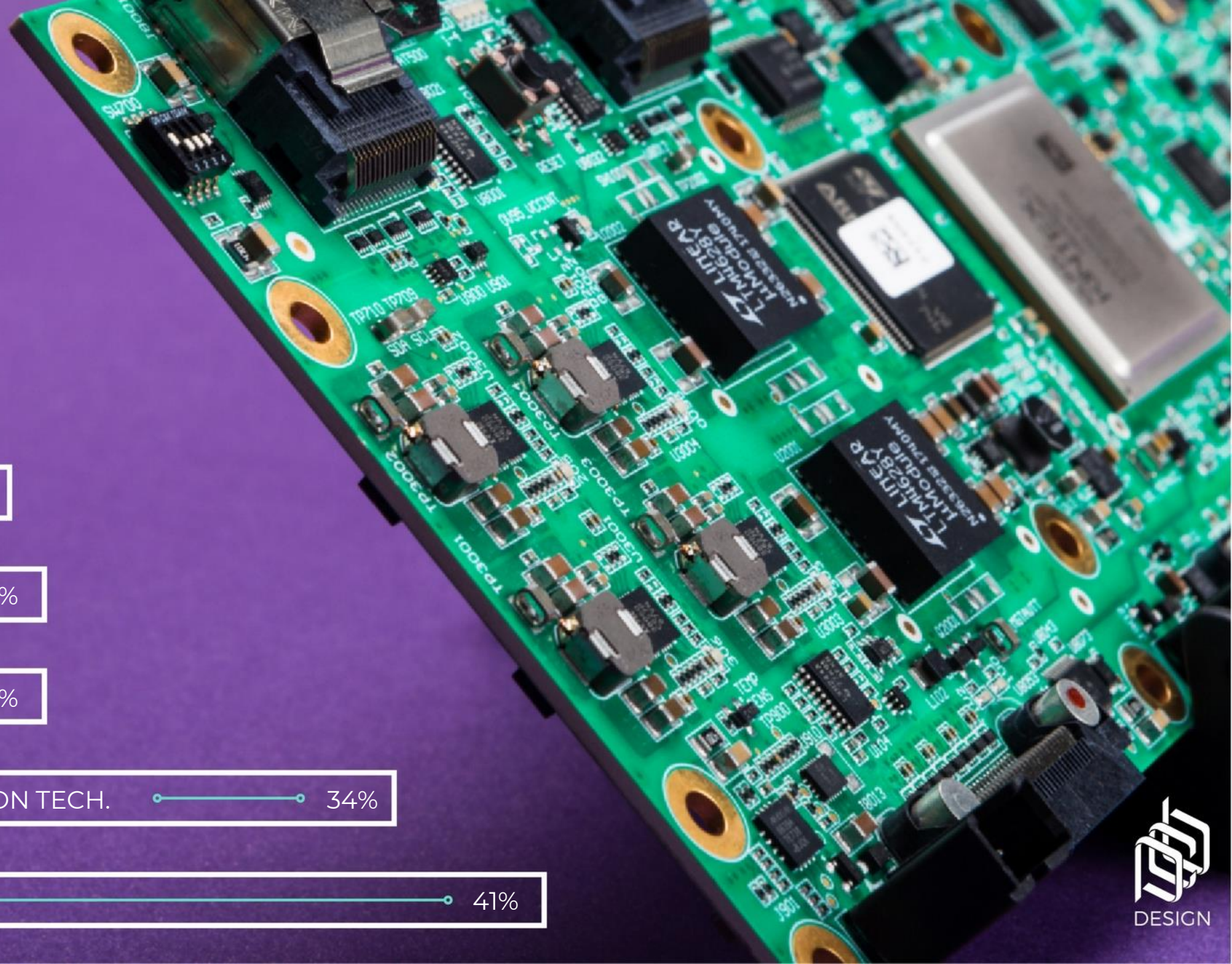
# WHO WE ARE

Engineering solution provider
- Major focus on high-speed PCBs
From concept to manufacturing
150 designs/year I 35+ engineers I 70+ customers

DESIGN
FROM CONCEPT TO MANUFACTURING

# INDUSTRIES & PARTNERS

- CONSUMER — 5%
- MEDICAL — 6%
- INDUSTRIAL — 7%
- AUTOMOTIVE — 7%
- INFORMATION & COMMUNICATION TECH. — 34%
- AEROSPACE & DEFENSE — 41%



DESIGN

# MARKETS

FINLAND

SWITZERLAND

GERMANY

ENGLAND

AUSTRALIA

NORWAY

BELGIUM

USA

IRELAND

ISRAEL

HUNGARY

DENMARK

DESIGN



# BRAINE Project

Active contribution in various projects

- **H2020**, Horizon Europe
- ESA
- Cascaded funding (TETRAMAX, Smart4All)
- EDF

*BRAINE: Big data Processing and Artificial Intelligence at the Network Edge*

H2020 ECSEL JU Grant No. 876967

https://www.braine-project.eu/

# EMDC Edge Micro Data Center


3.2 TB/s Ethernet switch


3 kW PSU

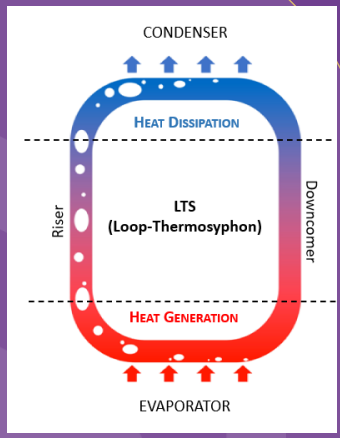

3U Enclosure for 8 compute nodes

**3U – Two phase cooled, 8/16/24 node EDGE /AI computer**

**Technology**

- **1.5 kW / 8 node**
- **Two phase passive cooling**

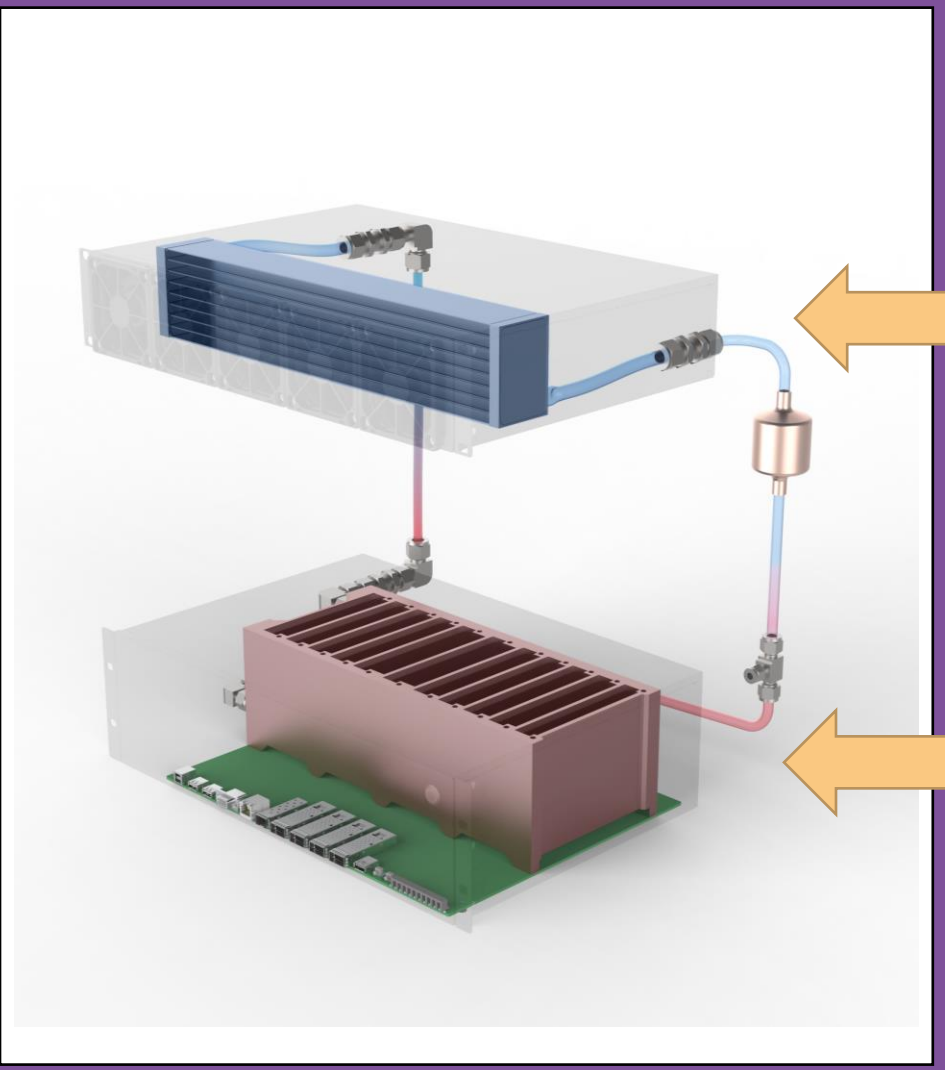
- Gen4 PCIe switch fabric
- 3.2 TB/s Ethernet switching (32 x 100G)
- 24 compute nodes in 3U
- 48V operation




**Node types**

- COM Express (Type VII ) CPU
- NVIDIA Xavier/Orin GPU
- Xilinx Versal AI FPGA
- 64 core ARM

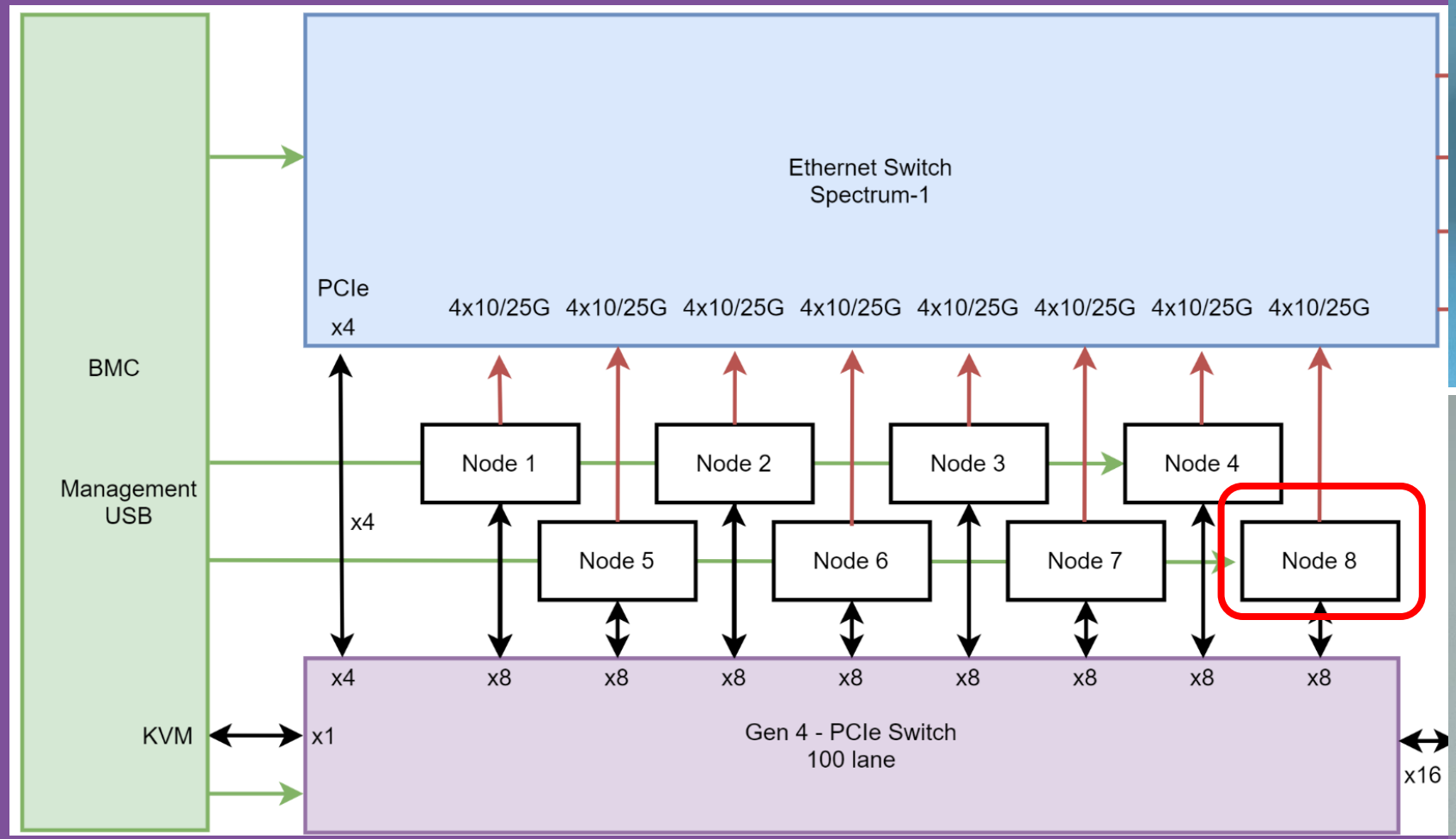
# EMDC Edge Micro Data Center



**Condenser Unit**

**Passive cooled Reconfigurable Server (EMDC)**

# EMDC - Basic architecture




AMD Epyc CPU
(COMe Type VII)

# Switch components

## Ethernet switch

- 128 x 25 G lane
- Mellanox / Spectrum 1
- 3.2 Tbit/sec switching
- 4x 100G External Ethernet
- 4x 25 G to each Node
- 26 layer stackup


Ethernet Switch

### PCIe Switch

- 96 lane Gen 4 PCIe Switching
- Each node - x8 interface

- 16 layer stackup

PCIe Switch

# Architectural simulations

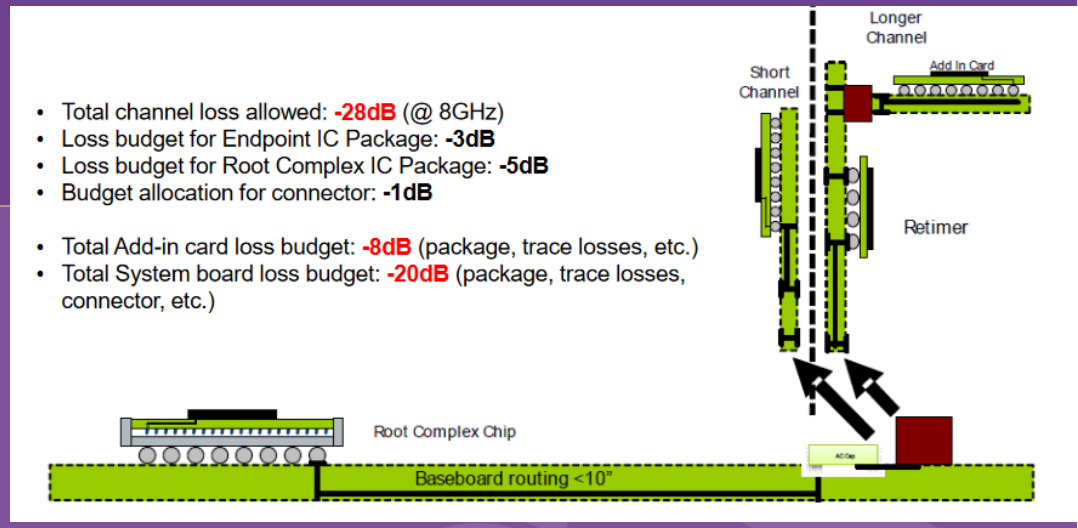
# Architecture simulations

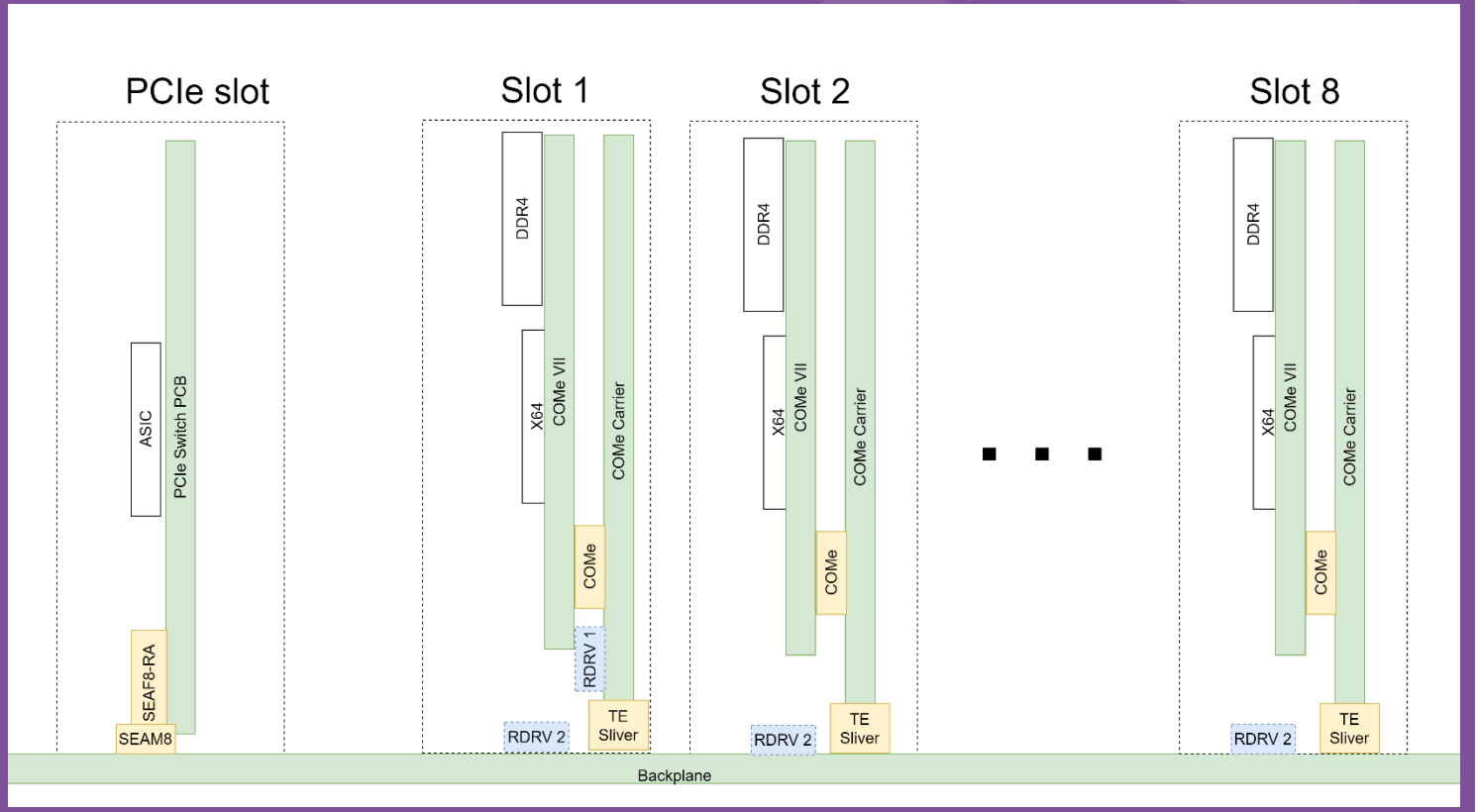
Should work with all Node types
- Com Express - Gen3
- GPU – Gen 4
- Dual connectors

Slot- slot distance
-Up to 300 mm

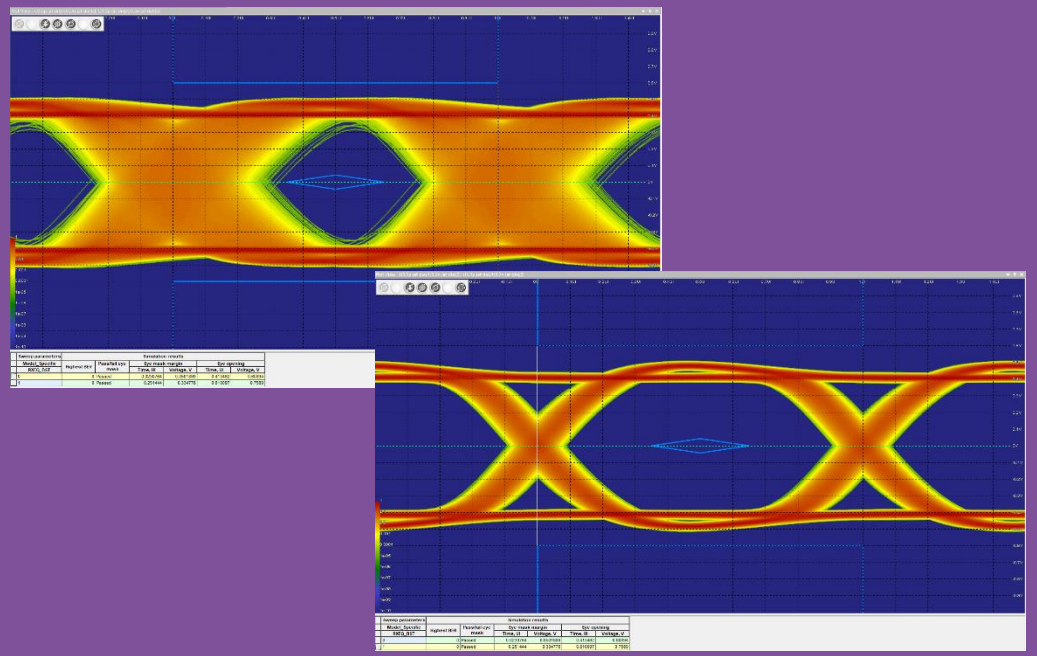
Connector Selection
PCB Material selection
-Channel Loss simulation

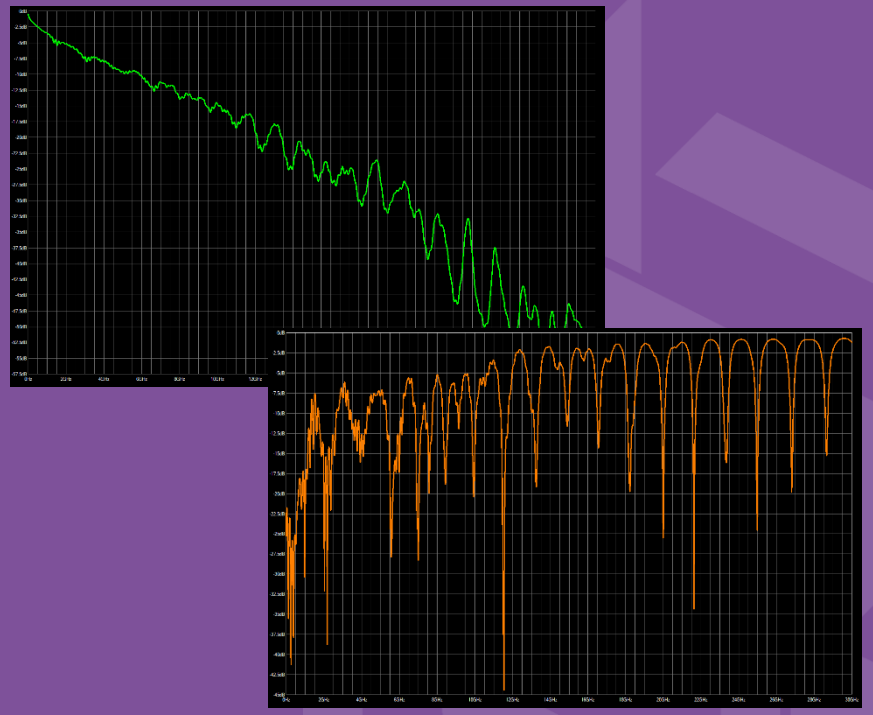
Re-driver required?
-If yes, where?

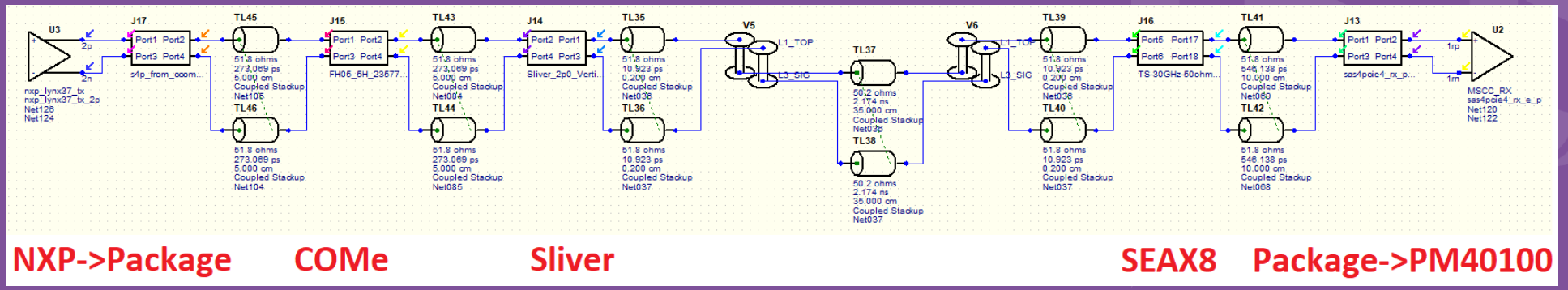


# Simulation results







# Conclusions

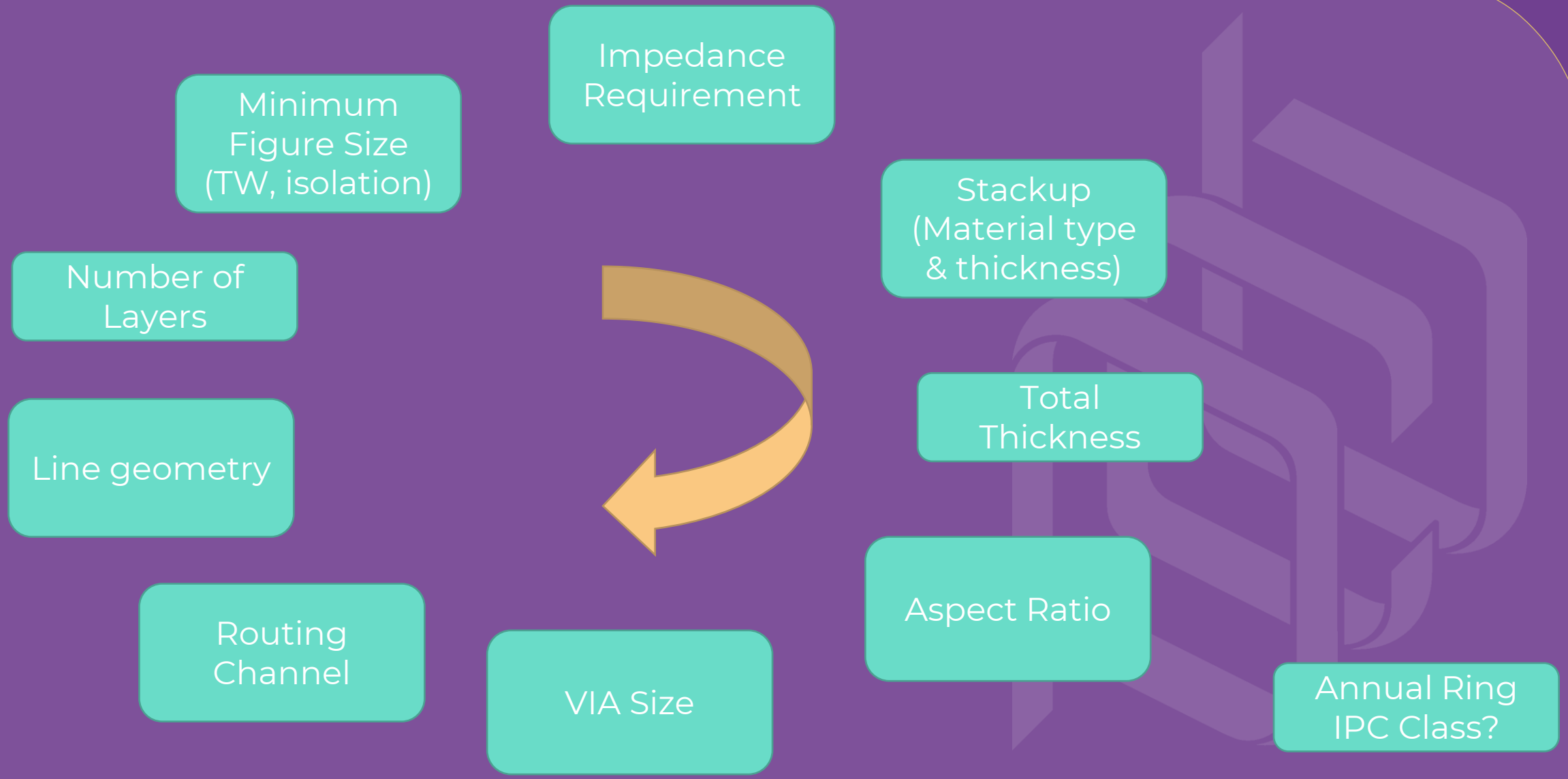
- Hard to find/trust simulation models
  - Com Express ?

- High Speed Material is required → MT40 was selected
- Backplane connector → ExaMax

- Re-timer/Repeater → Not required
  - 12 dB loss @ 8 GHz
  - If PCIe slot is in the middle

- “Universal” G-S-G structure stripline configuration

# Catch 22–High-Speed design parameters



# High Speed design
# Losses & Impedance match

- Resistive losses
  - Conductor DC resistance
  - Skin depth
  - **Surface roughness -> HVLP material**

- Dielectric loss
  - Dielectric loss exceeds resistive loss around 3 Gbit/s
  - Material selection (Df)
  - Conductor geometry (Dk) - **Loss vs. routability**
  - Signal dispersion due to different relative propagation delay
    - Df Stability
    - Prep-preg construction

# Stackup – VIA size

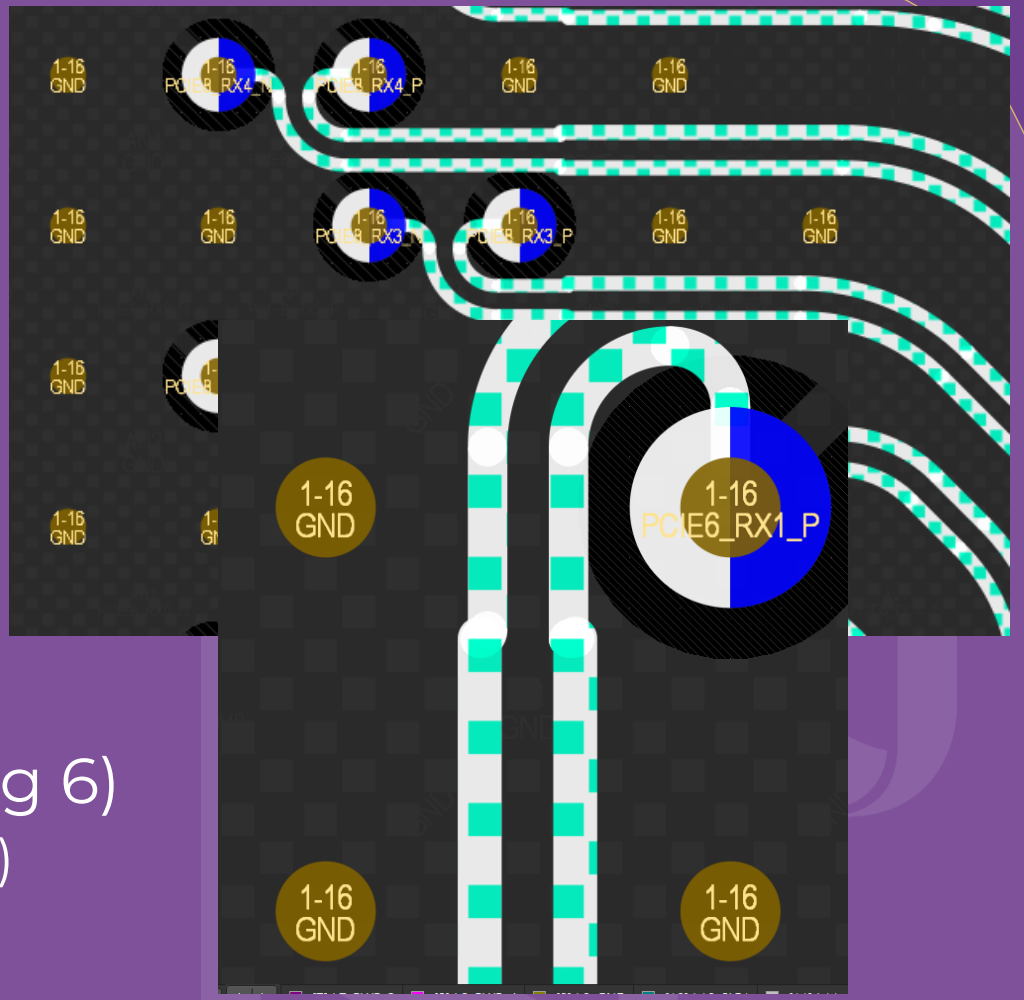
- Standard technology
  - Through via + microvia if required
  - No buried via if possible
- “Universal” G-S-G layer structure
  - Signal layer count is not defined yet
  - cca. 250 um (only) / signal layer
  - MT40-Dk-3.3
- Total thickness
  - Required number of signal (+power)  layers
  - If exceeding 1.6 mm
    - Card edge connector (Standard PCIe problem) →No problem here
  - If exceeding 2 mm
    - Pin length –>Press fit -> No problem
  - Aspect ratio 1:8 max 1:10
    - Results VIA size constraints

| | | | | |
|---|---|---|---|---|
| 13 | L13_GND | | Signal | 0.018mm |
| | Dielectric 9 | I-TERA_MT40-103... | Prepreg | 0.05mm |
| | Dielectric 5 | I-TERA_MT40-103... | Prepreg | 0.05mm |
| 14 | L14_SIG3 | | Signal | 0.018mm |
| | Dielectric 6 | ISOLA I-TERA MT-... | Core | 0.102mm |
| 15 | L15_GND | | Signal | 0.018mm |

# Fanout

- 1 mm BGA pitch
- Diff line fanout
- 1mm routing channel
  - 500 um PAD Size
    - 250 um drill size
      - 1:8 Aspect ratio @ 2mm PCB
      - 1:10 Aspect ratio @ 2.5mm PCB
    - 2 x 125 um annual ring

  - 500 um Routing channel – MT40(Meg 6)
    - Ideally 5x 100um (2 Signal + 3 separation)
    - DIFF 100: 85 um SIG + 0.11 GAP
    - **DIFF 85:  110um SIG + 125 um GAP**
      - **results 77 um drill to track**
      - **neckdown**




77 + (110 + 125 + 110) + 77

# Catch 22– Solution for High-Speed designs

DESIGN

Impedance Requirement

DIFF 100
DIFF 90, 85

"100um"
>75um

Minimum Figure Size (TW, isolation)

Stackup (Material type & thickness)

MT40
Megtron 6

Number of Layers

1.6 mm- 16 layers
2 mm – 20 layers

Total Thickness

1.6 mm
2 mm
2.5 mm
3 mm

Line geometry

"100/100um"
85/110um

Aspect Ratio

1:8
1:10

Routing Channel

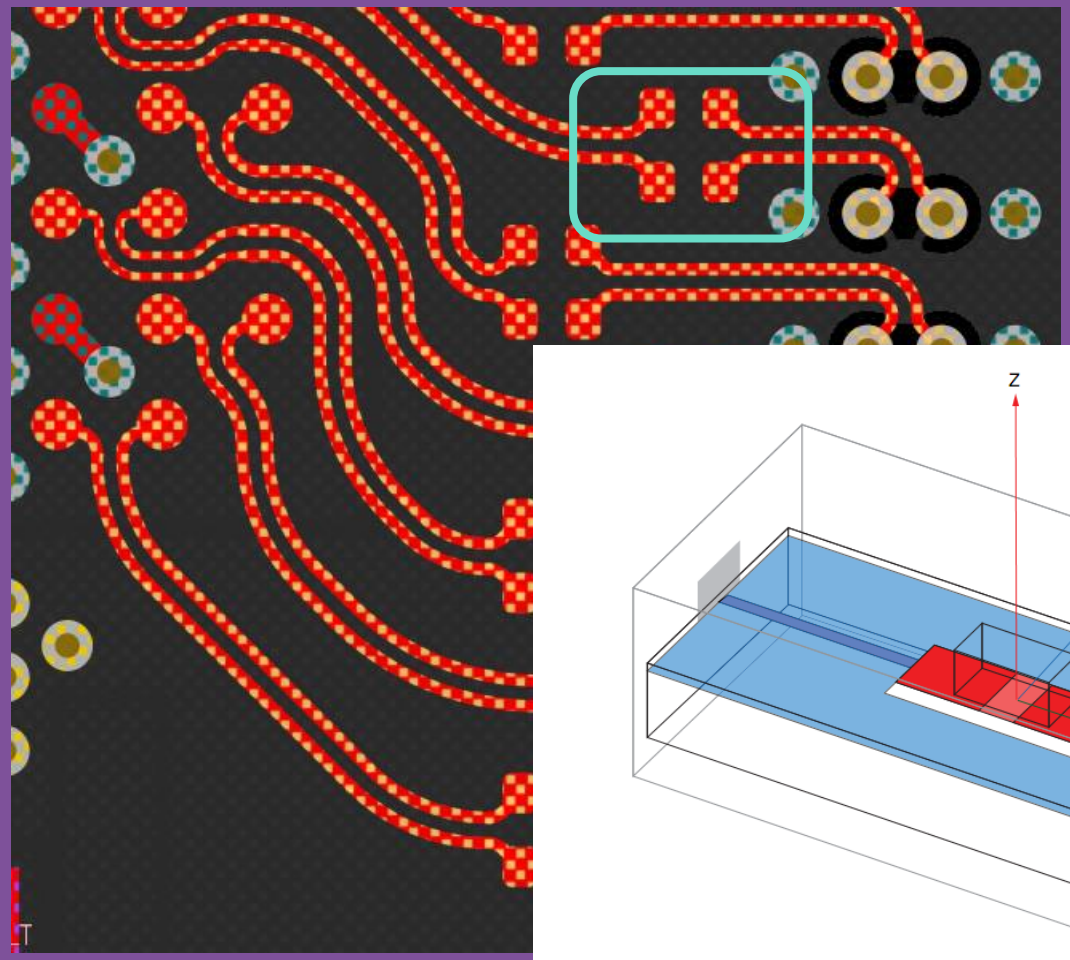
500 um

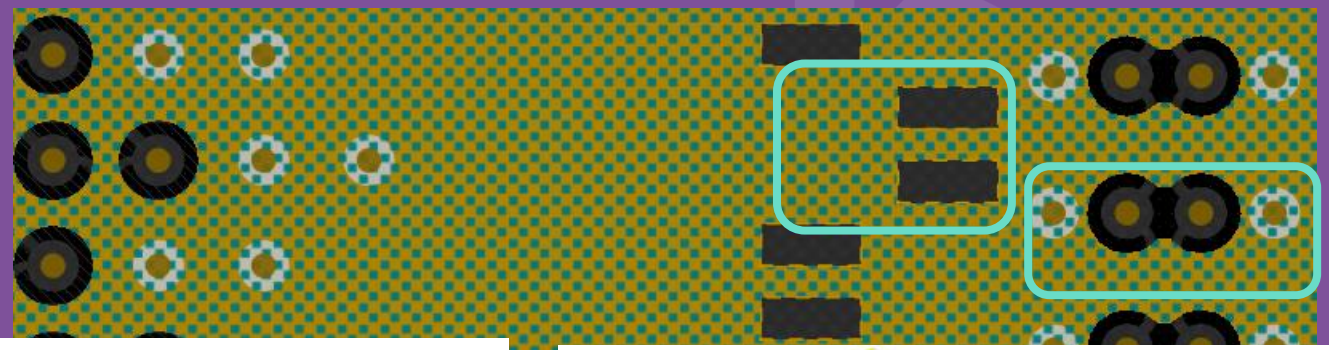
VIA Size

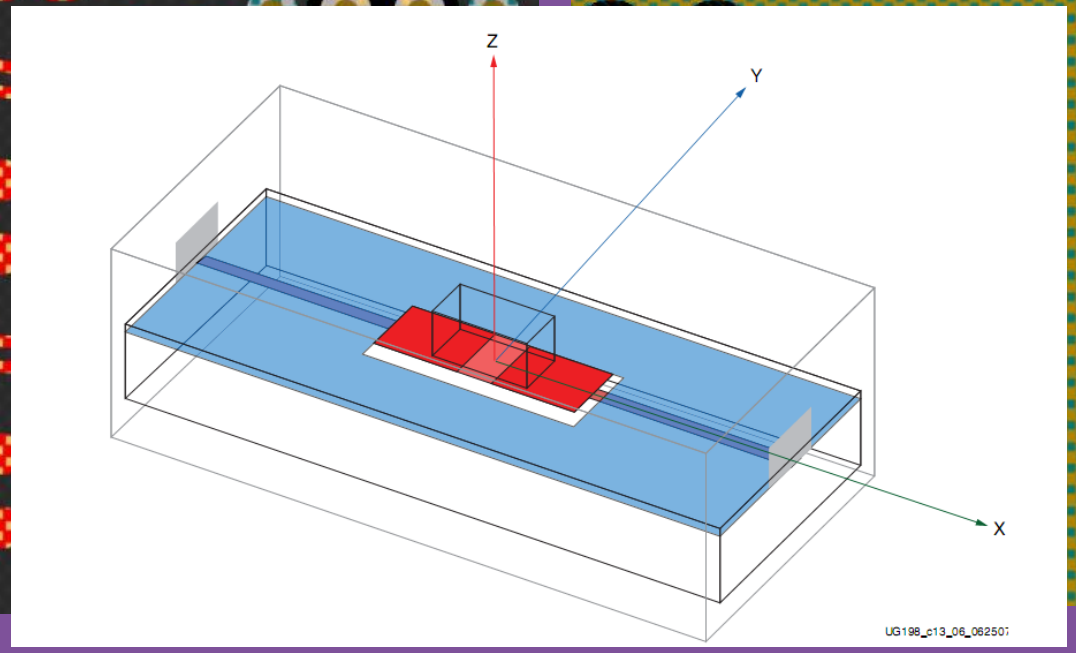
500um PAD
250 um Tool

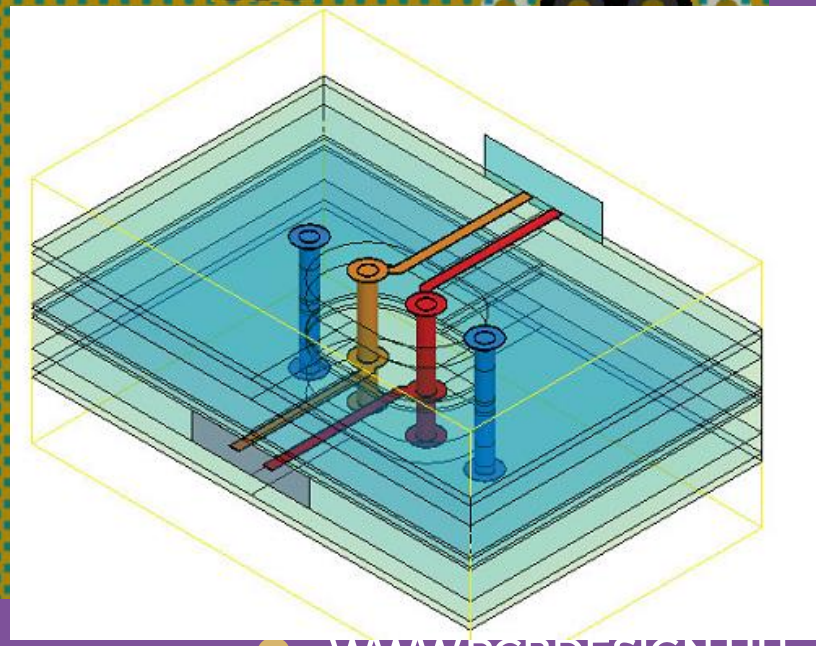
Annual Ring
IPC Class?

# Minimize impedance mismatch



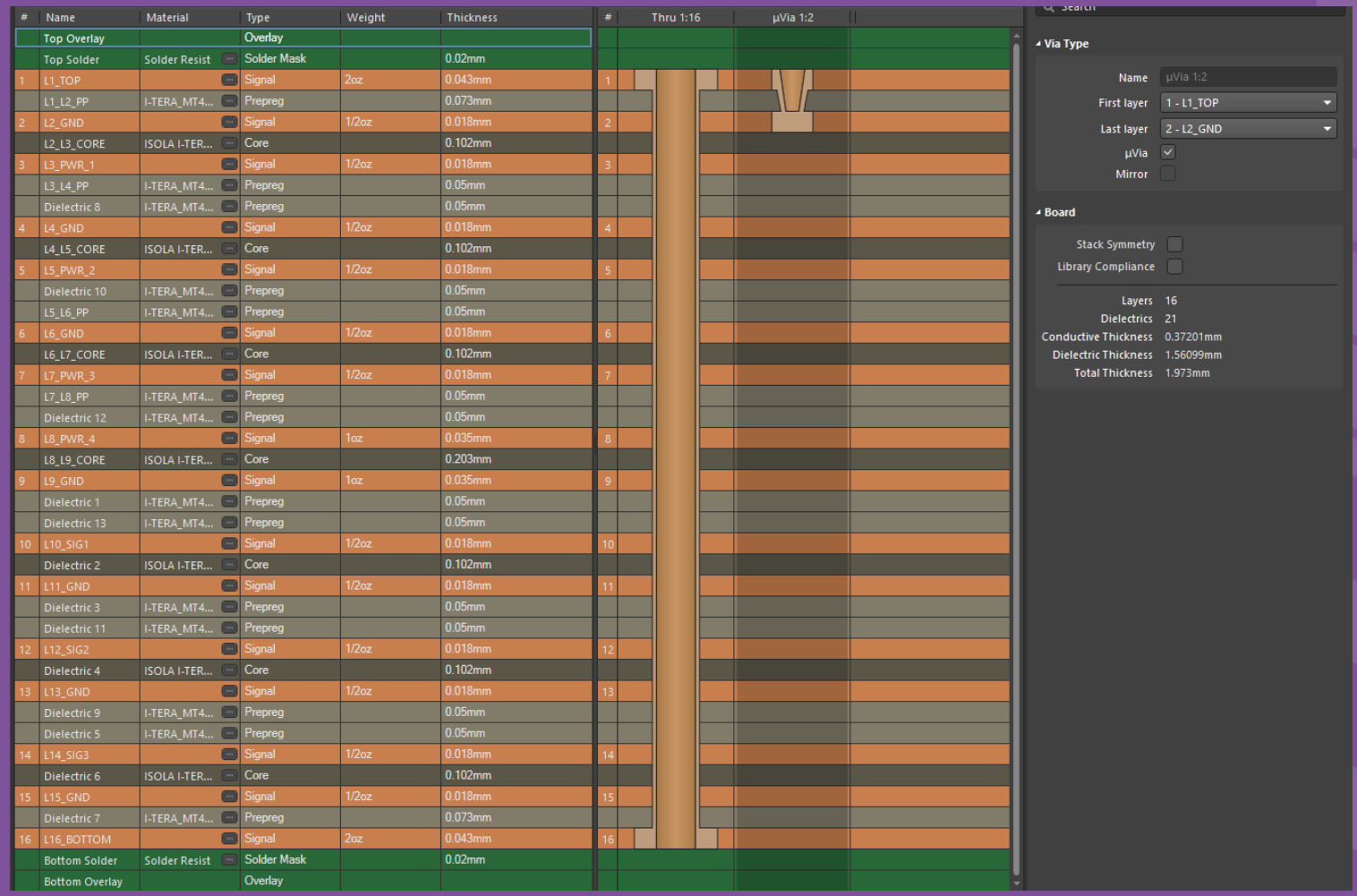




# Impedance - VIA setup

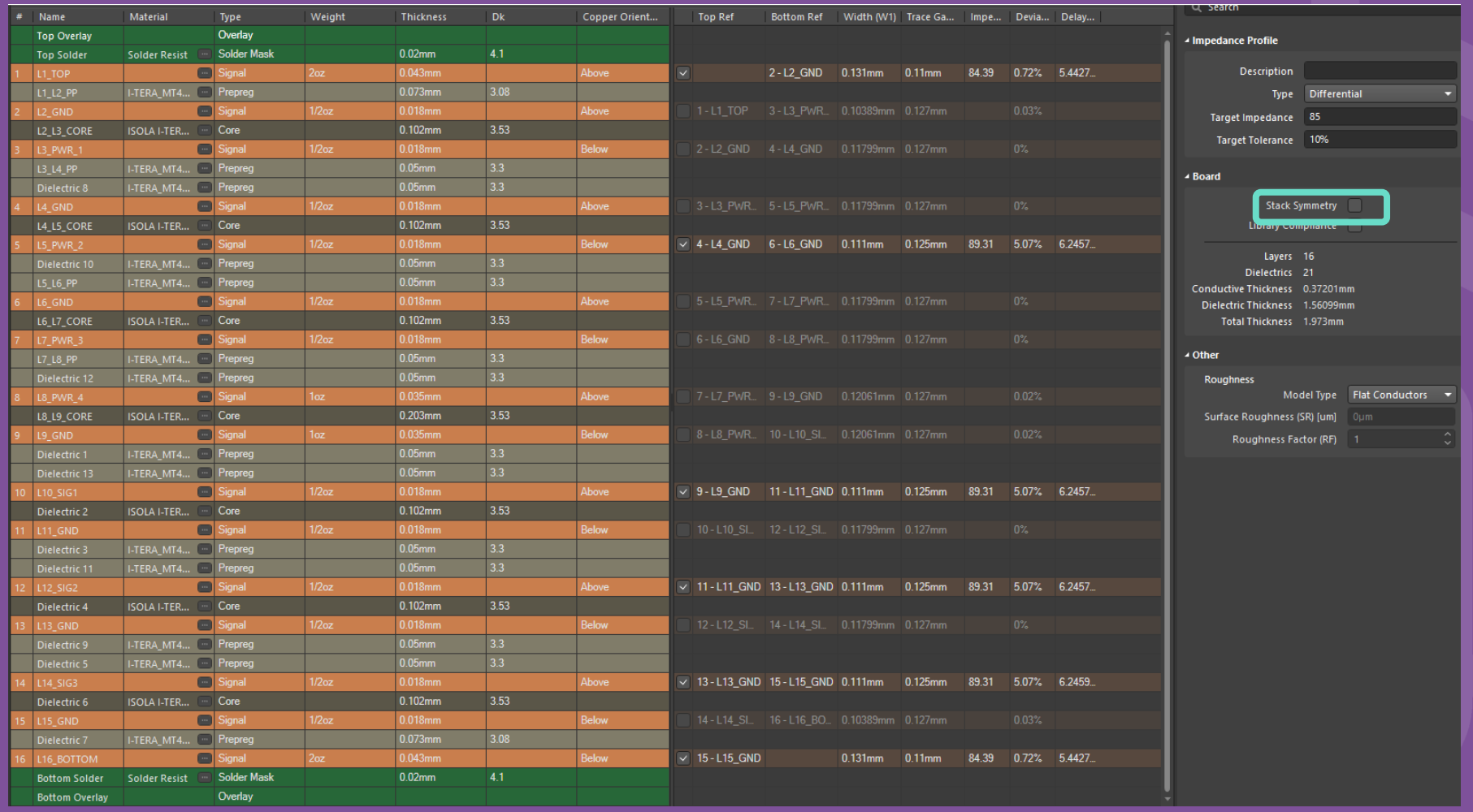
- Stackup and VIA settings



| # | Name | Material | Type | Weight | Thickness |
|---|---|---|---|---|---|
| | Top Overlay | | Overlay | | |
| | Top Solder | Solder Resist | Solder Mask | | 0.02mm |
| 1 | L1_TOP | | Signal | 2oz | 0.043mm |
| | L1_L2_PP | I-TERA_MT4... | Prepreg | | 0.073mm |
| 2 | L2_GND | | Signal | 1/2oz | 0.018mm |
| | L2_L3_CORE | ISOLA I-TER... | Core | | 0.102mm |
| 3 | L3_PWR_1 | | Signal | 1/2oz | 0.018mm |
| | L3_L4_PP | I-TERA_MT4... | Prepreg | | 0.05mm |
| | Dielectric 8 | I-TERA_MT4... | Prepreg | | 0.05mm |
| 4 | L4_GND | | Signal | 1/2oz | 0.018mm |
| | L4_L5_CORE | ISOLA I-TER... | Core | | 0.102mm |
| 5 | L5_PWR_2 | | Signal | 1/2oz | 0.018mm |
| | Dielectric 10 | I-TERA_MT4... | Prepreg | | 0.05mm |
| | L5_L6_PP | I-TERA_MT4... | Prepreg | | 0.05mm |
| 6 | L6_GND | | Signal | 1/2oz | 0.018mm |
| | L6_L7_CORE | ISOLA I-TER... | Core | | 0.102mm |
| 7 | L7_PWR_3 | | Signal | 1/2oz | 0.018mm |
| | L7_L8_PP | I-TERA_MT4... | Prepreg | | 0.05mm |
| | Dielectric 12 | I-TERA_MT4... | Prepreg | | 0.05mm |
| 8 | L8_PWR_4 | | Signal | 1oz | 0.035mm |
| | L8_L9_CORE | ISOLA I-TER... | Core | | 0.203mm |
| 9 | L9_GND | | Signal | 1oz | 0.035mm |
| | Dielectric 1 | I-TERA_MT4... | Prepreg | | 0.05mm |
| | Dielectric 13 | I-TERA_MT4... | Prepreg | | 0.05mm |
| 10 | L10_SIG1 | | Signal | 1/2oz | 0.018mm |
| | Dielectric 2 | ISOLA I-TER... | Core | | 0.102mm |
| 11 | L11_GND | | Signal | 1/2oz | 0.018mm |
| | Dielectric 3 | I-TERA_MT4... | Prepreg | | 0.05mm |
| | Dielectric 11 | I-TERA_MT4... | Prepreg | | 0.05mm |
| 12 | L12_SIG2 | | Signal | 1/2oz | 0.018mm |
| | Dielectric 4 | ISOLA I-TER... | Core | | 0.102mm |
| 13 | L13_GND | | Signal | 1/2oz | 0.018mm |
| | Dielectric 9 | I-TERA_MT4... | Prepreg | | 0.05mm |
| | Dielectric 5 | I-TERA_MT4... | Prepreg | | 0.05mm |
| 14 | L14_SIG3 | | Signal | 1/2oz | 0.018mm |
| | Dielectric 6 | ISOLA I-TER... | Core | | 0.102mm |
| 15 | L15_GND | | Signal | 1/2oz | 0.018mm |
| | Dielectric 7 | I-TERA_MT4... | Prepreg | | 0.073mm |
| 16 | L16_BOTTOM | | Signal | 2oz | 0.043mm |
| | Bottom Solder | Solder Resist | Solder Mask | | 0.02mm |
| | Bottom Overlay | | Overlay | | |

# Impedance - VIA setup

- Impedance table



| # | Name | Material | Type | Weight | Thickness | Dk | Copper Orient... |
|---|---|---|---|---|---|---|---|
| | Top Overlay | | Overlay | | | | |
| | Top Solder | Solder Resist | Solder Mask | | 0.02mm | 4.1 | |
| 1 | L1_TOP | | Signal | 2oz | 0.043mm | | Above |
| | L1_L2_PP | I-TERA_MT4... | Prepreg | | 0.073mm | 3.08 | |
| 2 | L2_GND | | Signal | 1/2oz | 0.018mm | | Above |
| | L2_L3_CORE | ISOLA I-TER... | Core | | 0.102mm | 3.53 | |
| 3 | L3_PWR_1 | | Signal | 1/2oz | 0.018mm | | Below |
| | L3_L4_PP | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| | Dielectric 8 | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| 4 | L4_GND | | Signal | 1/2oz | 0.018mm | | Above |
| | L4_L5_CORE | ISOLA I-TER... | Core | | 0.102mm | 3.53 | |
| 5 | L5_PWR_2 | | Signal | 1/2oz | 0.018mm | | Below |
| | Dielectric 10 | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| | L5_L6_PP | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| 6 | L6_GND | | Signal | 1/2oz | 0.018mm | | Above |
| | L6_L7_CORE | ISOLA I-TER... | Core | | 0.102mm | 3.53 | |
| 7 | L7_PWR_3 | | Signal | 1/2oz | 0.018mm | | Below |
| | L7_L8_PP | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| | Dielectric 12 | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| 8 | L8_PWR_4 | | Signal | 1oz | 0.035mm | | Above |
| | L8_L9_CORE | ISOLA I-TER... | Core | | 0.203mm | 3.53 | |
| 9 | L9_GND | | Signal | 1oz | 0.035mm | | Below |
| | Dielectric 1 | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| | Dielectric 13 | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| 10 | L10_SIG1 | | Signal | 1/2oz | 0.018mm | | Above |
| | Dielectric 2 | ISOLA I-TER... | Core | | 0.102mm | 3.53 | |
| 11 | L11_GND | | Signal | 1/2oz | 0.018mm | | Below |
| | Dielectric 3 | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| | Dielectric 11 | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| 12 | L12_SIG2 | | Signal | 1/2oz | 0.018mm | | Above |
| | Dielectric 4 | ISOLA I-TER... | Core | | 0.102mm | 3.53 | |
| 13 | L13_GND | | Signal | 1/2oz | 0.018mm | | Below |
| | Dielectric 9 | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| | Dielectric 5 | I-TERA_MT4... | Prepreg | | 0.05mm | 3.3 | |
| 14 | L14_SIG3 | | Signal | 1/2oz | 0.018mm | | Above |
| | Dielectric 6 | ISOLA I-TER... | Core | | 0.102mm | 3.53 | |
| 15 | L15_GND | | Signal | 1/2oz | 0.018mm | | Below |
| | Dielectric 7 | I-TERA_MT4... | Prepreg | | 0.073mm | 3.08 | |
| 16 | L16_BOTTOM | | Signal | 2oz | 0.043mm | | Below |
| | Bottom Solder | Solder Resist | Solder Mask | | 0.02mm | 4.1 | |
| | Bottom Overlay | | Overlay | | | | |

| Top Ref | Bottom Ref | Width (W1) | Trace Ga... | Impe... | Devia... | Delay... |
|---|---|---|---|---|---|---|
| | 2 - L2_GND | 0.131mm | 0.11mm | 84.39 | 0.72% | 5.4427... |
| 1 - L1_TOP | 3 - L3_PWR... | 0.10389mm | 0.127mm | | 0.03% | |
| 2 - L2_GND | 4 - L4_GND | 0.11799mm | 0.127mm | | 0% | |
| 3 - L3_PWR... | 5 - L5_PWR... | 0.11799mm | 0.127mm | | 0% | |
| 4 - L4_GND | 6 - L6_GND | 0.111mm | 0.125mm | 89.31 | 5.07% | 6.2457... |
| 5 - L5_PWR... | 7 - L7_PWR... | 0.11799mm | 0.127mm | | 0% | |
| 6 - L6_GND | 8 - L8_PWR... | 0.11799mm | 0.127mm | | 0% | |
| 7 - L7_PWR... | 9 - L9_GND | 0.12061mm | 0.127mm | | 0.02% | |
| 8 - L8_PWR... | 10 - L10_SI... | 0.12061mm | 0.127mm | | 0.02% | |
| 9 - L9_GND | 11 - L11_GND | 0.111mm | 0.125mm | 89.31 | 5.07% | 6.2457... |
| 10 - L10_SI... | 12 - L12_SI... | 0.11799mm | 0.127mm | | 0% | |
| 11 - L11_GND | 13 - L13_GND | 0.111mm | 0.125mm | 89.31 | 5.07% | 6.2457... |
| 12 - L12_SI... | 14 - L14_SI... | 0.11799mm | 0.127mm | | 0% | |
| 13 - L13_GND | 15 - L15_GND | 0.111mm | 0.125mm | 89.31 | 5.07% | 6.2459... |
| 14 - L14_SI... | 16 - L16_BO... | 0.10389mm | 0.127mm | | 0.03% | |
| 15 - L15_GND | | 0.131mm | 0.11mm | 84.39 | 0.72% | 5.4427... |

Search

**Impedance Profile**

Description
Type: Differential
Target Impedance: 85
Target Tolerance: 10%

**Board**

Stack Symmetry
Library Compliance

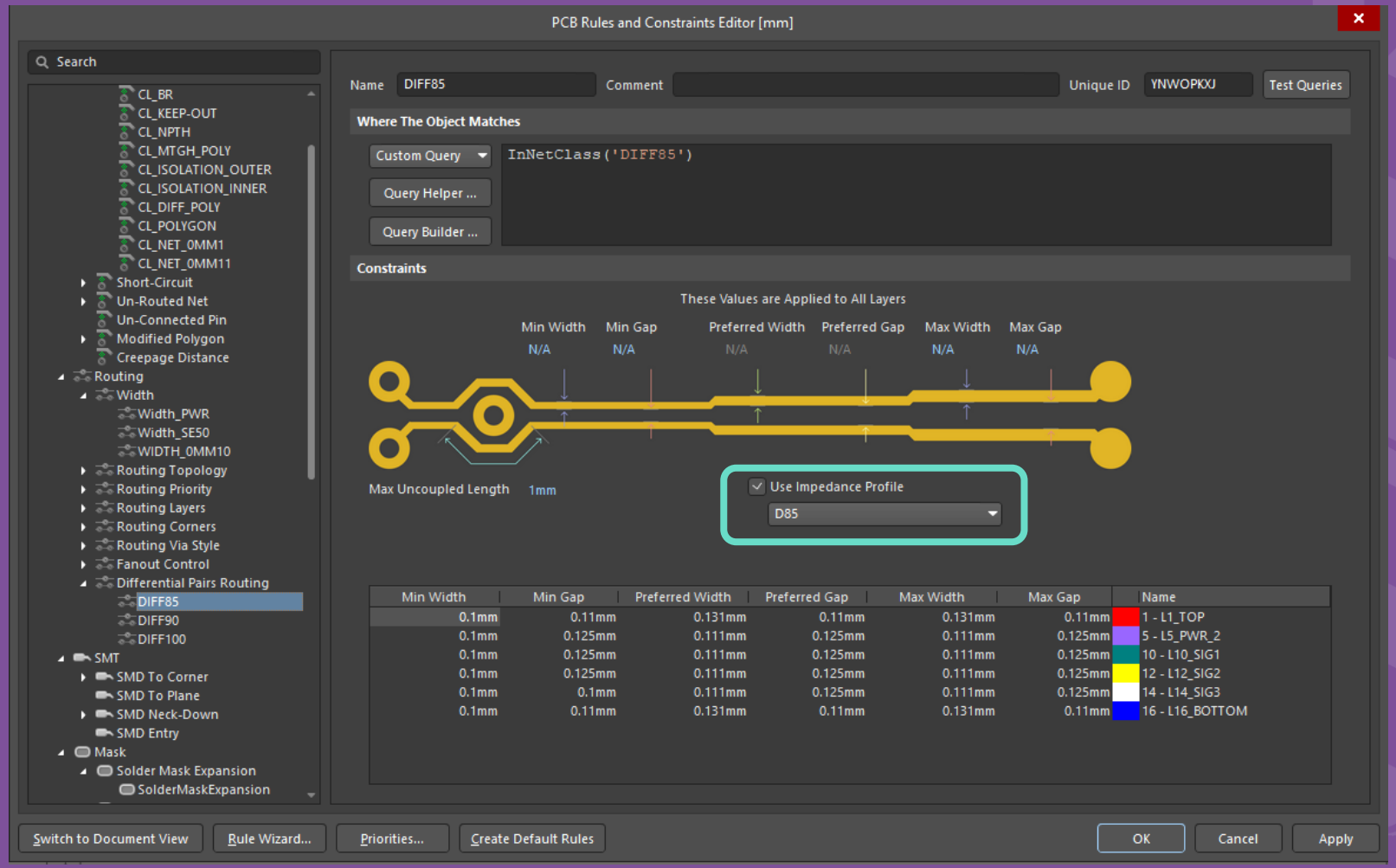
Layers: 16
Dielectrics: 21
Conductive Thickness: 0.37201mm
Dielectric Thickness: 1.56099mm
Total Thickness: 1.973mm

**Other**

Roughness
Model Type: Flat Conductors
Surface Roughness (SR) [um]: 0µm
Roughness Factor (RF): 1

# Impedance - VIA setup

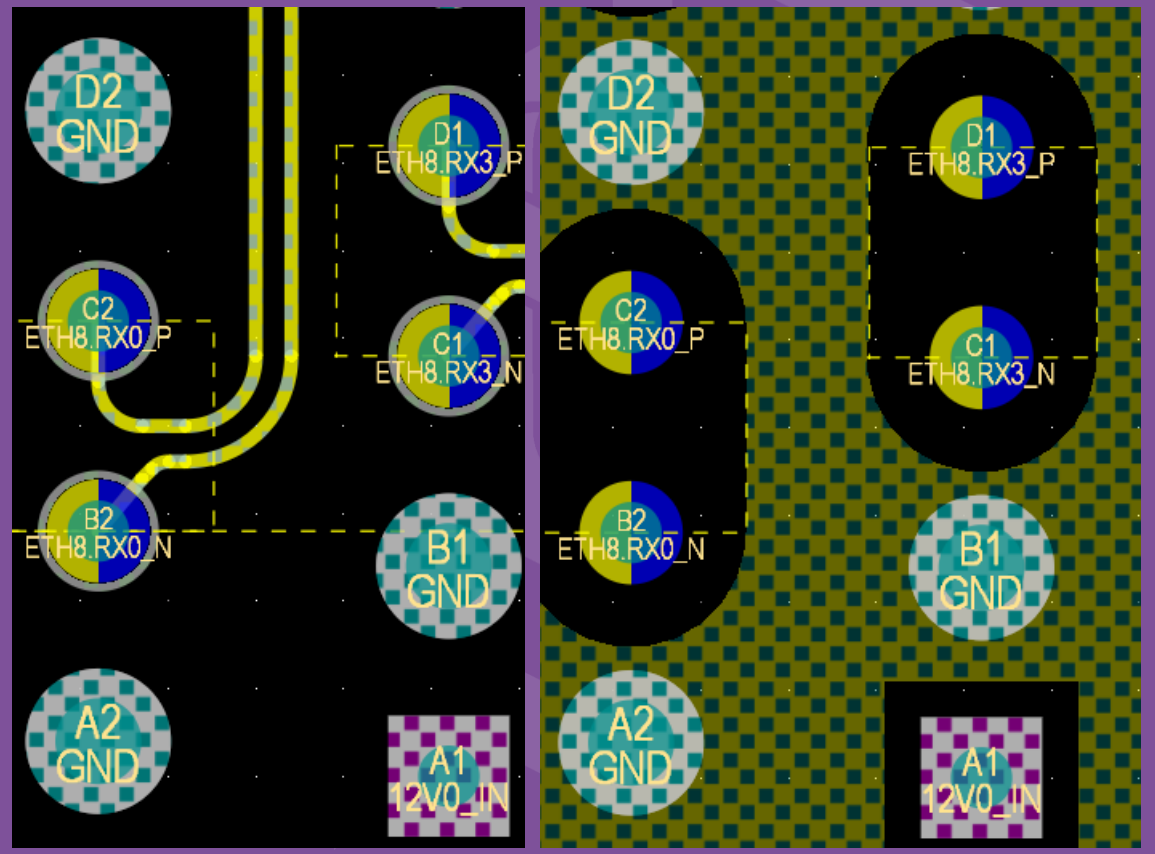
- Impedance – net class, rule



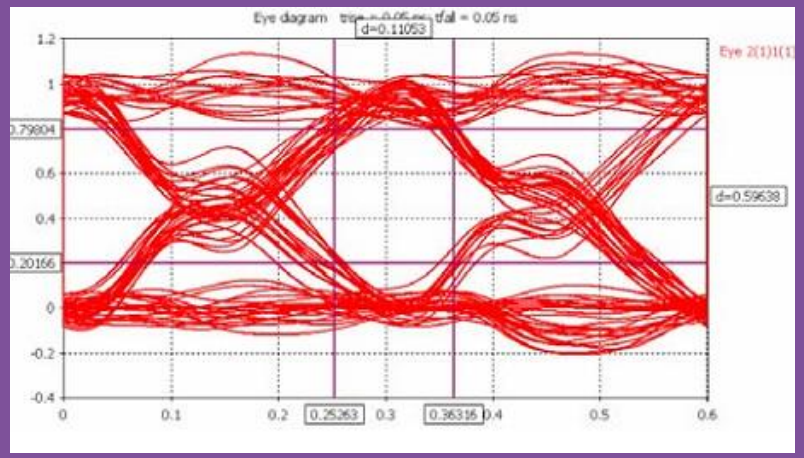
# Advanced topics

# Additional items to consider

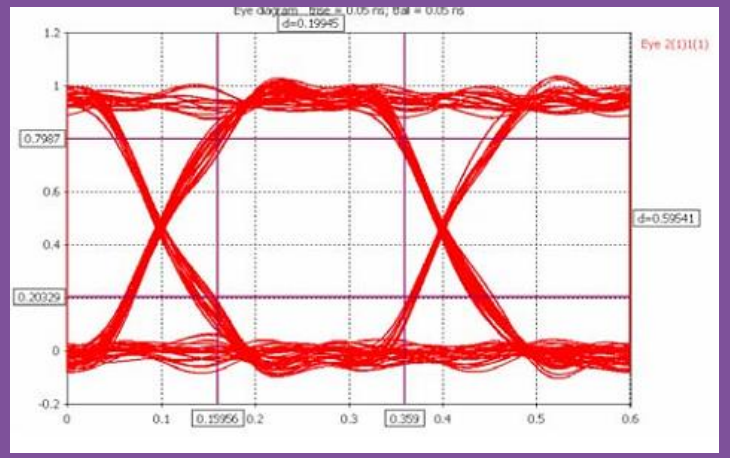
- Examax routing
  - Antipad design
  - Length equalization wo. serpentine
  - Backdrill depth limit



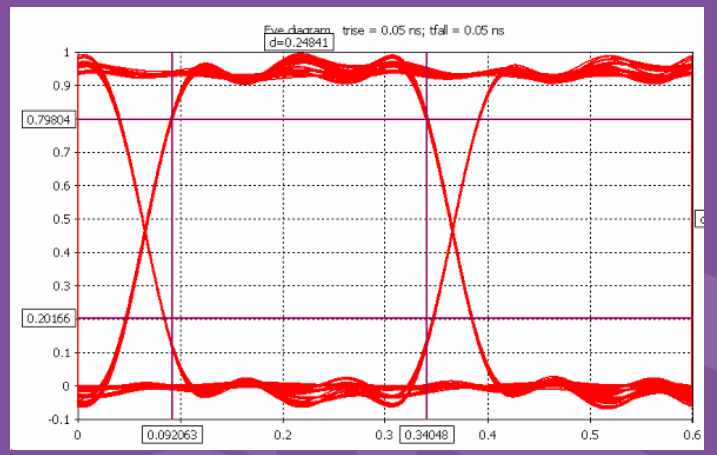
# Back drilling –stub effect




3.3 mm Stub

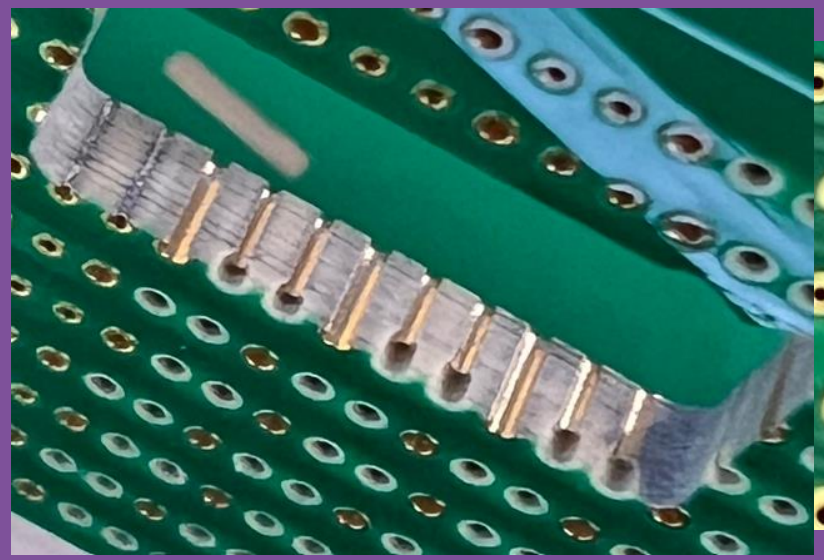


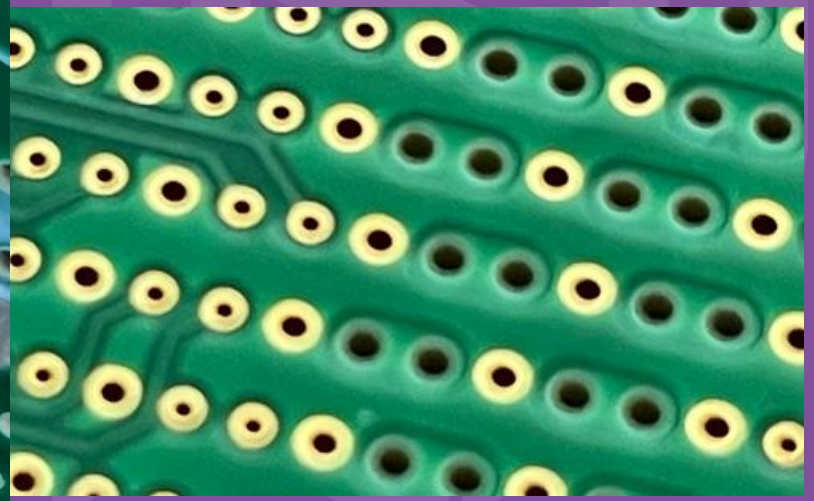

1.35 mm Stub




No Stub

- 16 layer PCB
- VIA L1-L2
- 50ps rise/fall time
- 300ps pulse



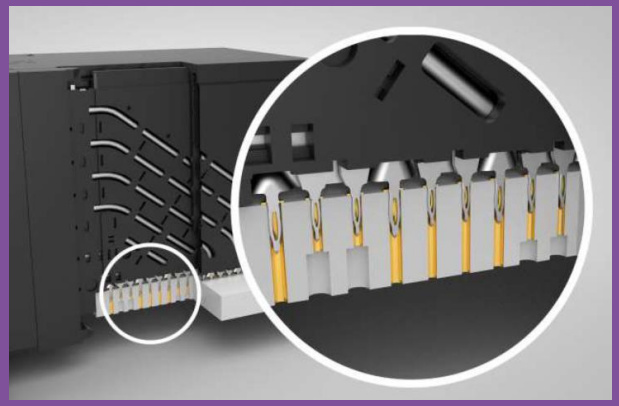


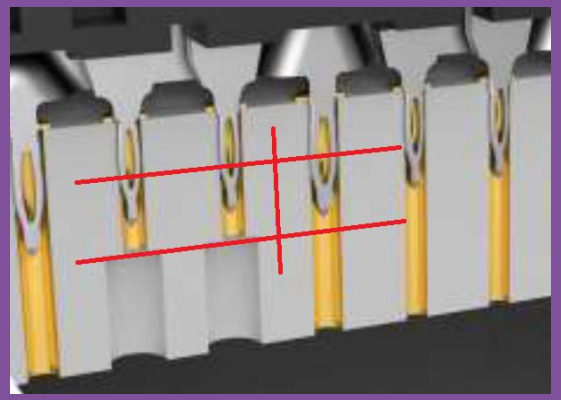


http://www.basebandhub.com/pdfs/viastubs.pdf

# Additional items to consider

- **Press-fit + drill tolerance limitation**



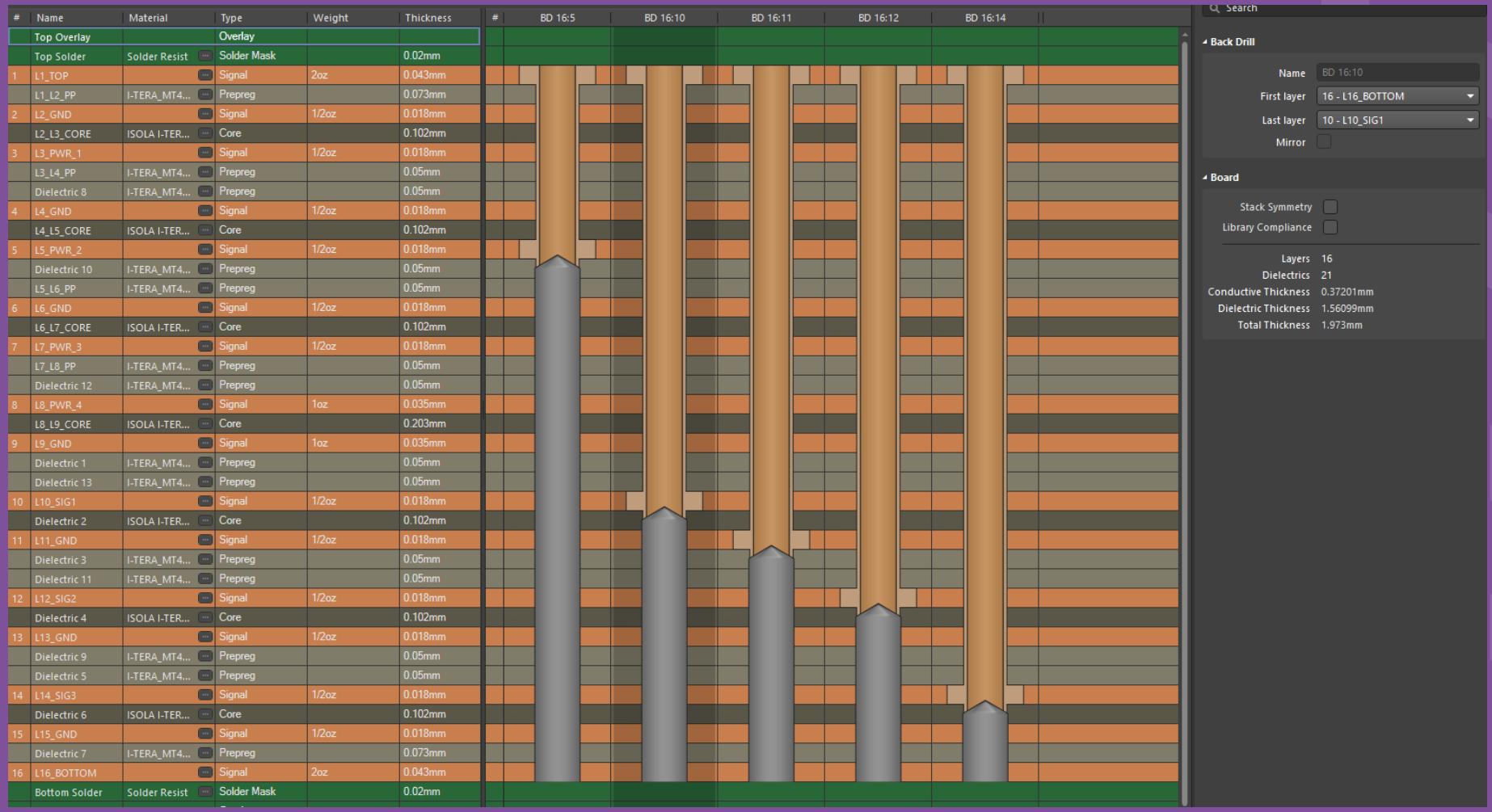


- Topmost layers still suffer  from stub

- Altium does not recognize press fit

# Backdrill setup in Altium

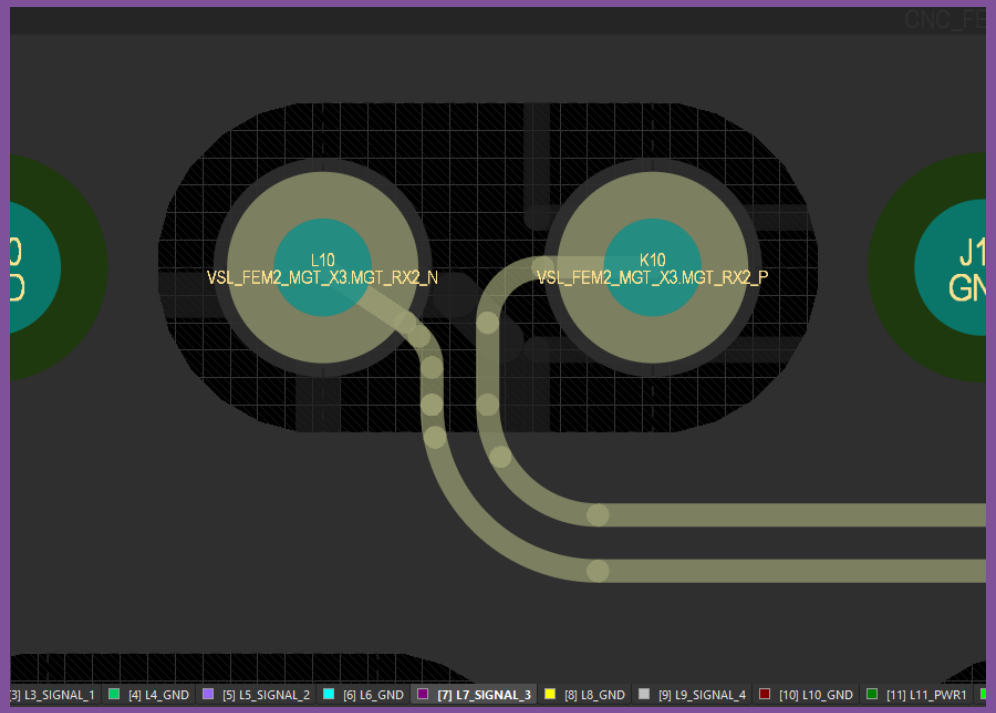
- Automatically generated after setup
- .

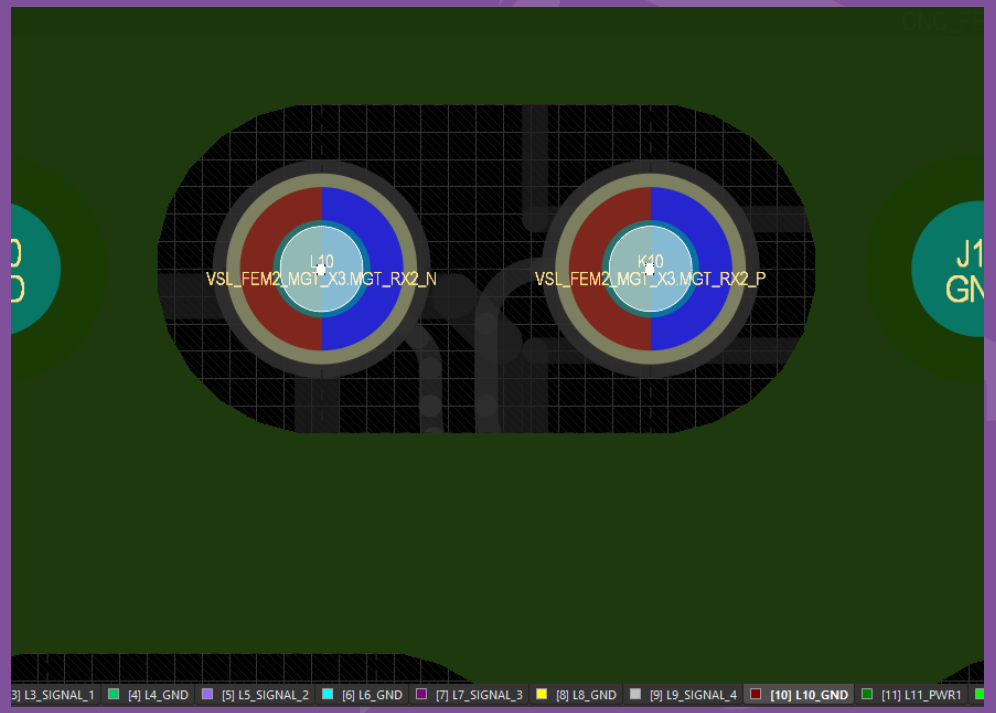


| # | Name | Material | Type | Weight | Thickness |
|---|---|---|---|---|---|
| | Top Overlay | | Overlay | | |
| | Top Solder | Solder Resist | Solder Mask | | 0.02mm |
| 1 | L1_TOP | | Signal | 2oz | 0.043mm |
| | L1_L2_PP | I-TERA_MT4... | Prepreg | | 0.073mm |
| 2 | L2_GND | | Signal | 1/2oz | 0.018mm |
| | L2_L3_CORE | ISOLA I-TER... | Core | | 0.102mm |
| 3 | L3_PWR_1 | | Signal | 1/2oz | 0.018mm |
| | L3_L4_PP | I-TERA_MT4... | Prepreg | | 0.05mm |
| | Dielectric 8 | I-TERA_MT4... | Prepreg | | 0.05mm |
| 4 | L4_GND | | Signal | 1/2oz | 0.018mm |
| | L4_L5_CORE | ISOLA I-TER... | Core | | 0.102mm |
| 5 | L5_PWR_2 | | Signal | 1/2oz | 0.018mm |
| | Dielectric 10 | I-TERA_MT4... | Prepreg | | 0.05mm |
| | L5_L6_PP | I-TERA_MT4... | Prepreg | | 0.05mm |
| 6 | L6_GND | | Signal | 1/2oz | 0.018mm |
| | L6_L7_CORE | ISOLA I-TER... | Core | | 0.102mm |
| 7 | L7_PWR_3 | | Signal | 1/2oz | 0.018mm |
| | L7_L8_PP | I-TERA_MT4... | Prepreg | | 0.05mm |
| | Dielectric 12 | I-TERA_MT4... | Prepreg | | 0.05mm |
| 8 | L8_PWR_4 | | Signal | 1oz | 0.035mm |
| | L8_L9_CORE | ISOLA I-TER... | Core | | 0.203mm |
| 9 | L9_GND | | Signal | 1oz | 0.035mm |
| | Dielectric 1 | I-TERA_MT4... | Prepreg | | 0.05mm |
| | Dielectric 13 | I-TERA_MT4... | Prepreg | | 0.05mm |
| 10 | L10_SIG1 | | Signal | 1/2oz | 0.018mm |
| | Dielectric 2 | ISOLA I-TER... | Core | | 0.102mm |
| 11 | L11_GND | | Signal | 1/2oz | 0.018mm |
| | Dielectric 3 | I-TERA_MT4... | Prepreg | | 0.05mm |
| | Dielectric 11 | I-TERA_MT4... | Prepreg | | 0.05mm |
| 12 | L12_SIG2 | | Signal | 1/2oz | 0.018mm |
| | Dielectric 4 | ISOLA I-TER... | Core | | 0.102mm |
| 13 | L13_GND | | Signal | 1/2oz | 0.018mm |
| | Dielectric 9 | I-TERA_MT4... | Prepreg | | 0.05mm |
| | Dielectric 5 | I-TERA_MT4... | Prepreg | | 0.05mm |
| 14 | L14_SIG3 | | Signal | 1/2oz | 0.018mm |
| | Dielectric 6 | ISOLA I-TER... | Core | | 0.102mm |
| 15 | L15_GND | | Signal | 1/2oz | 0.018mm |
| | Dielectric 7 | I-TERA_MT4... | Prepreg | | 0.073mm |
| 16 | L16_BOTTOM | | Signal | 2oz | 0.043mm |
| | Bottom Solder | Solder Resist | Solder Mask | | 0.02mm |

# Backdrill setup in Altium

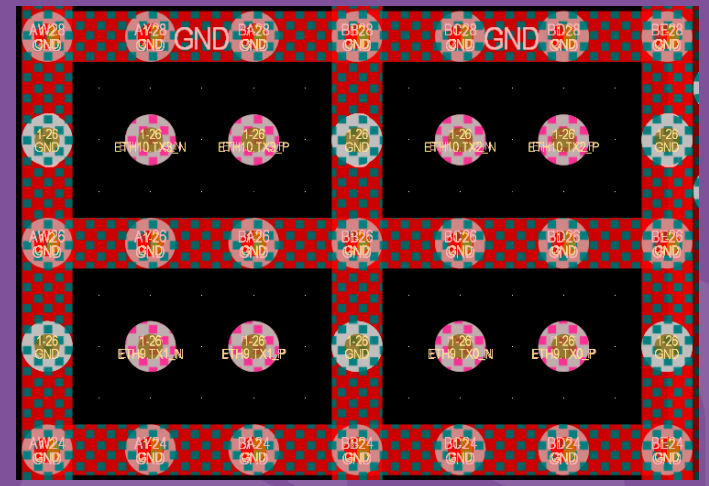
- Small feature to stop backdrill at press-fit.
  - Signal is routed on L7 -> backdrill would be automatically generated from bottom to L7.
  - Solution: add a small track to L10



# Additional items to consider

- Crosstalk mitigation
- Guard ring around the signals.
- VIA in PAD required.
  - IPC 4761 VII - Filled & Capped via




# Q & A

DESIGN

WWW.PCBDESIGN.HU

3 days training @ Budapest:
08 - 10 / March 2023