Mastering Design for Excellence(DFx) in High-Speed PCB Design: Achieving success in Signal Integrity and Manufacturability

DESIGN

FROM CONCEPT
TO MANUFACTURING

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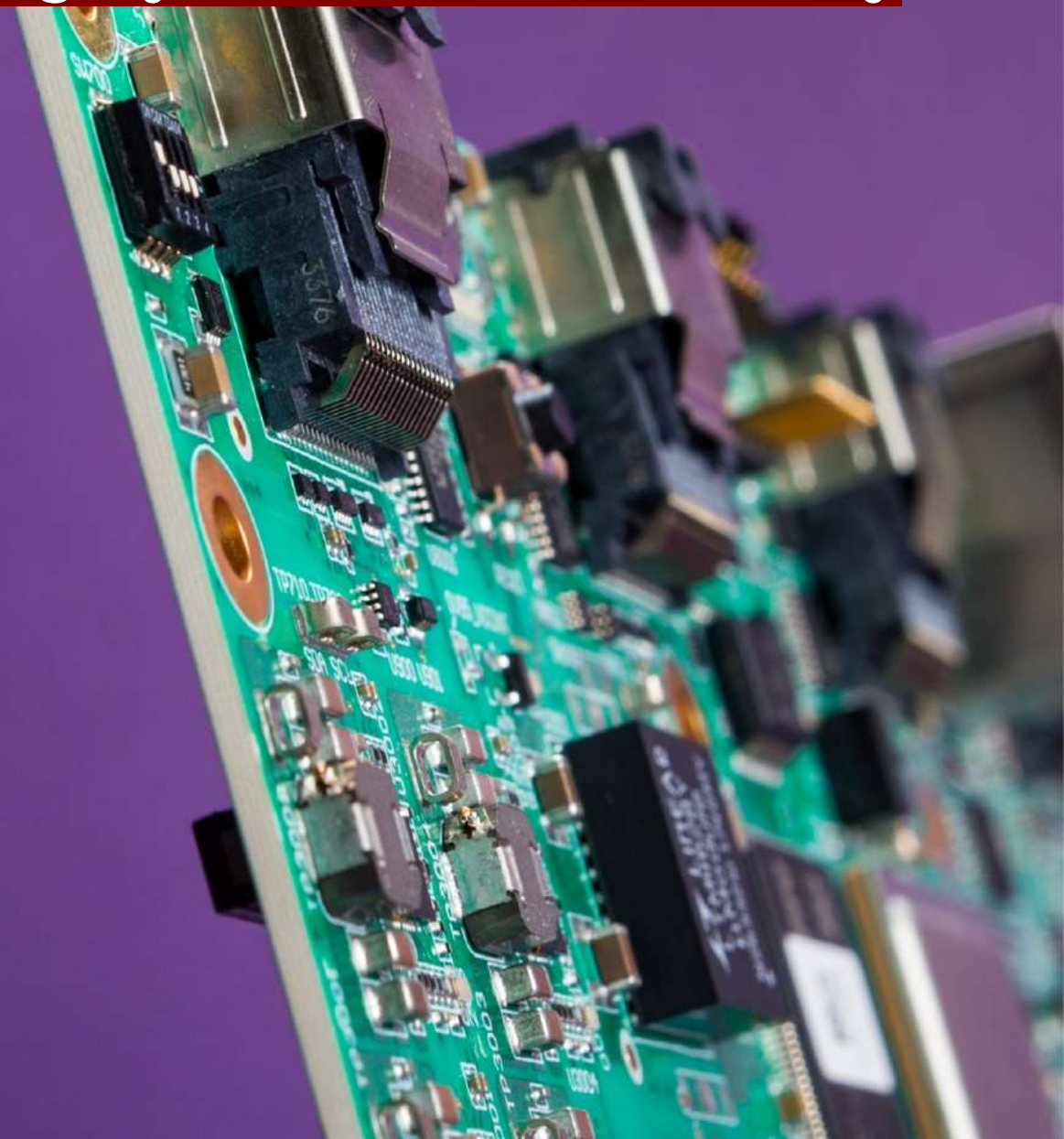


János Lazányi – CEO – PCB Design Kft.


WHO
WE ARE
Engineering solution provider
- Major focus on high-speed PCBs
From concept to manufacturing
150 designs/year I 35+ engineers I 70+ customers
DESIGN
FROM CONCEPT
TO MANUFACTURING

MARKETS

FINLAND

SWITZERLAND

GERMANY

ENGLAND

AUSTRALIA

NORWAY

BELGIUM

USA

IRELAND

ISRAEL

HUNGARY

DENMARK

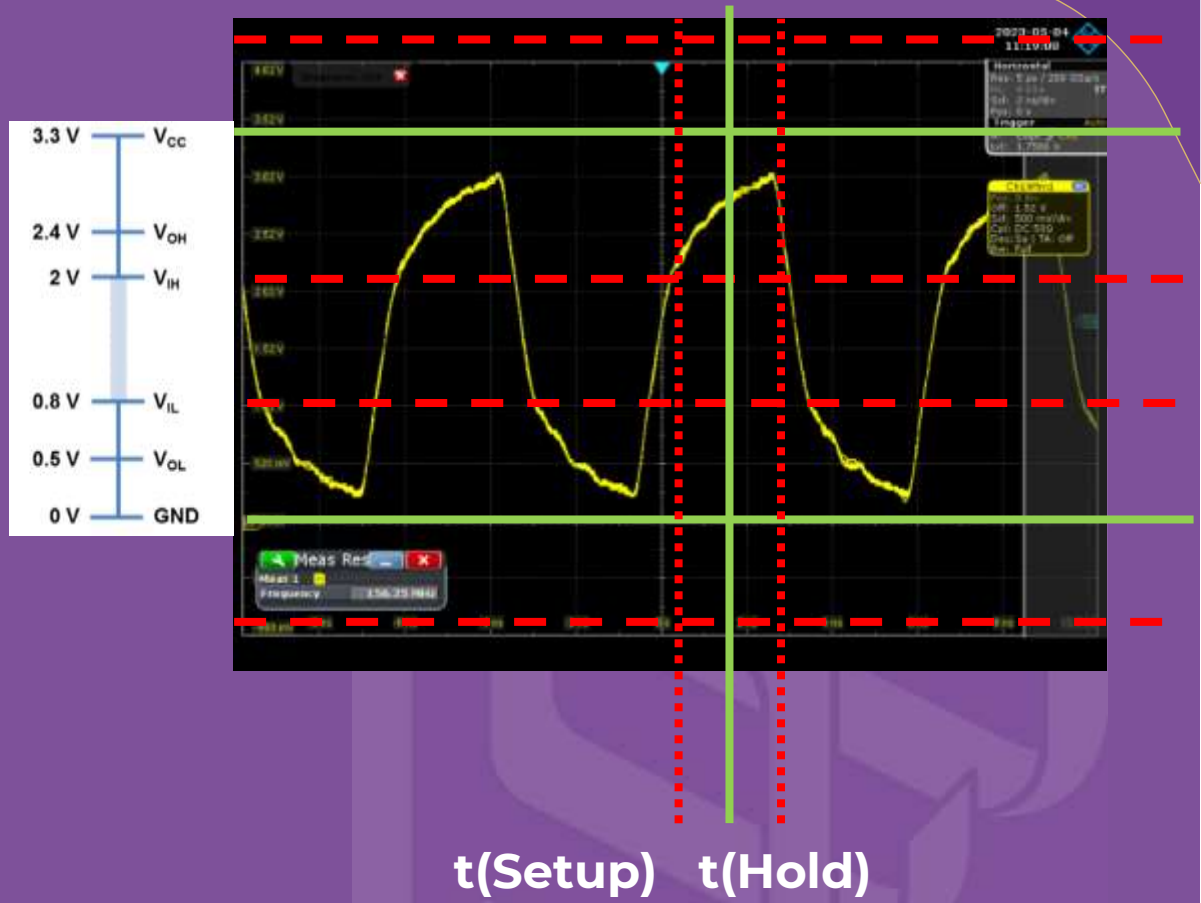
DESIGN

The purpose of Signal Integrity

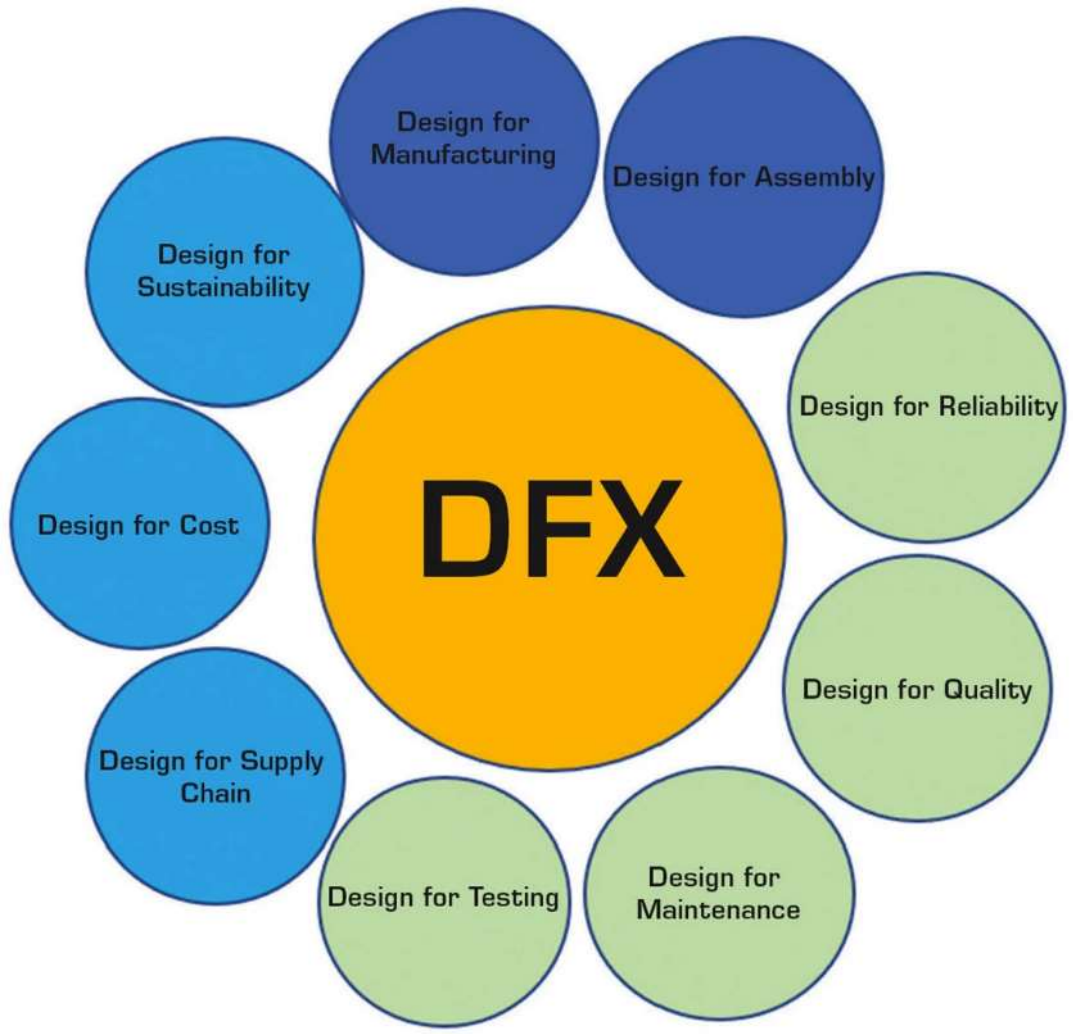
- SI: Ensuring signals can be interpreted **by the receiver.**
  - Amplitude &
  - Time Domain

- Sources of signal degradation
  - Impedance mismatch
  - Frequency response variation
  - Crosstalk
  - Noise

- Moreover:
  - Ensure Power Integrity
    - Ground Bounce & SSN
  - Ensure low EMI emission



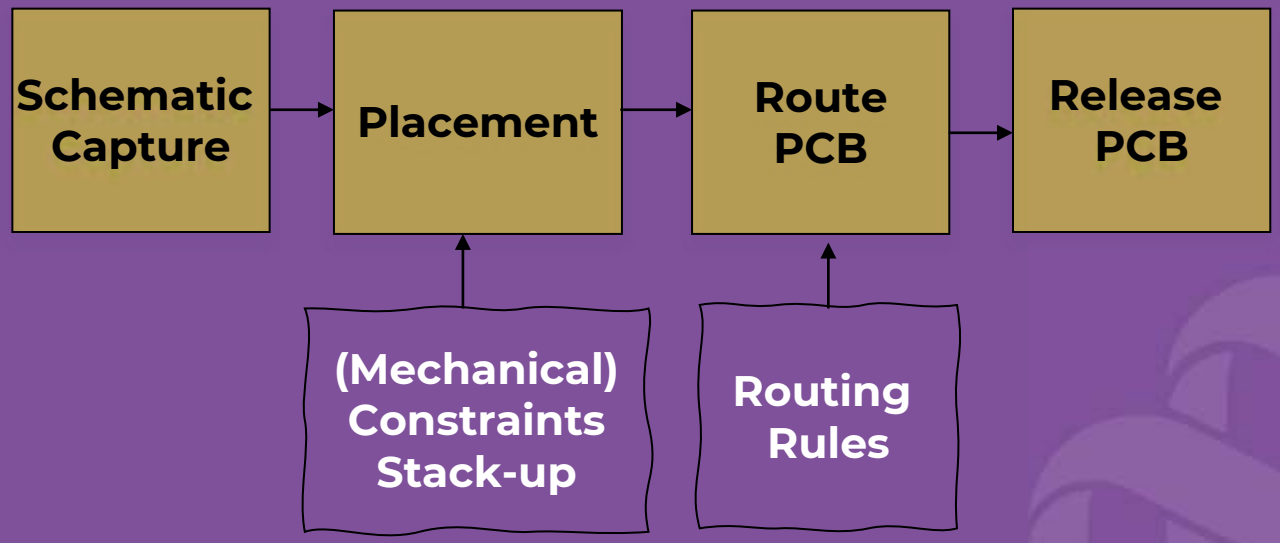
DFx in Nutshell



- Design for manufacturing (DFM)
- Design for assembly (DFA)
- Design for test (DFT)

- Design for quality (DFQ)
- Design for cost (DFC)

Typical PCB Design Flow



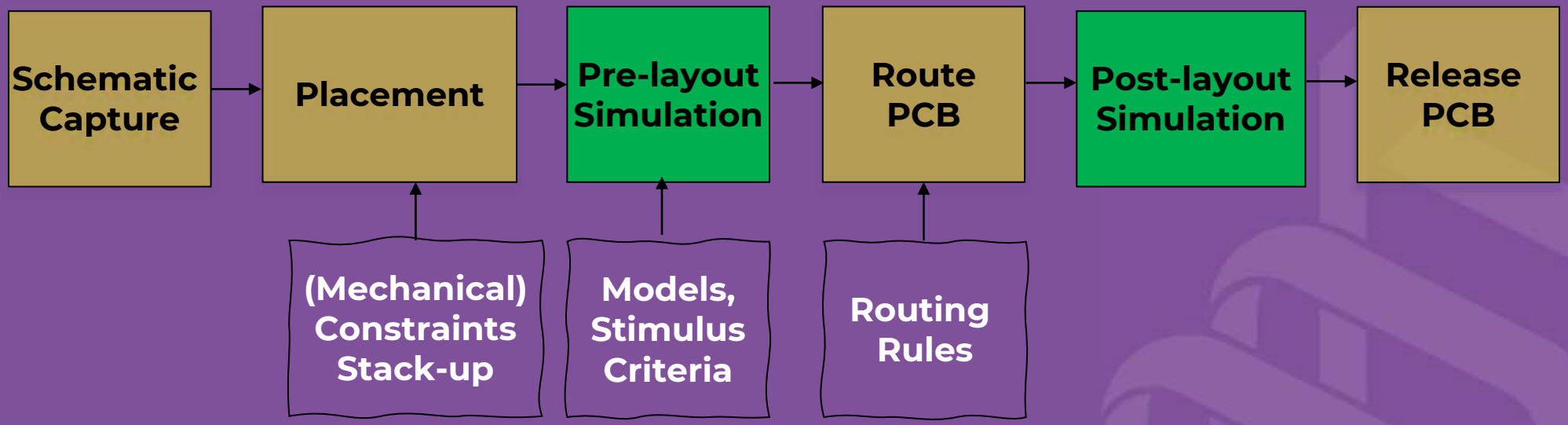
Design for manufacturing (DFM)

- Track/Via Geometry
- Edge Clearance
- Acid Traps
- Solder Mask Problems (Small pitch components)
- Via Problems (e.g. Placing Vias in Pads)

Design for assembly (DFA)

- Part-to Part Spacing
- Proper Footprint
- Solderability (Thumb stone)
- Reflow profile mismatch
- Used component technologies
  - SMT, THT, Press-fit
- One vs two sided PCB

Signal Integrity PCB Design Flow

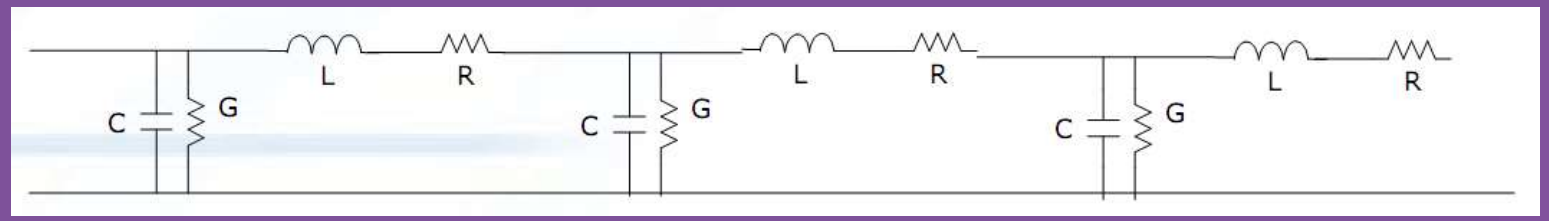


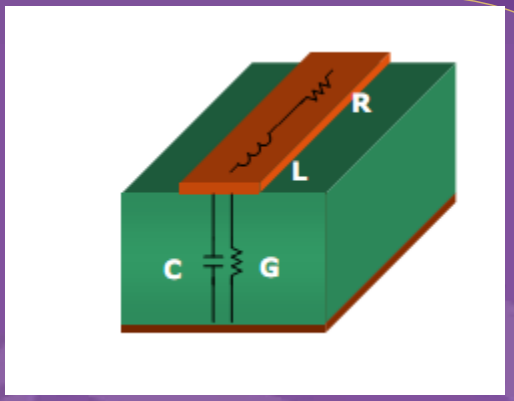
Design for Signal Integrity

- Material selection → loss
- Stackup → impedance mismatch & loss
- Track geometry → impedance mismatch & loss & cross-talk
- Topology →reflection

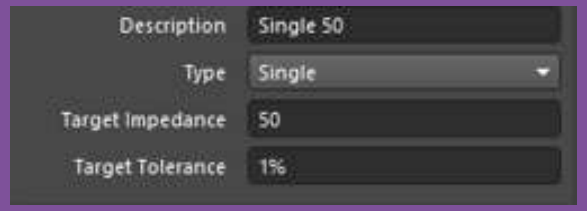
Loss optimalization of various track geometries

Transmission line & characteristic impedance



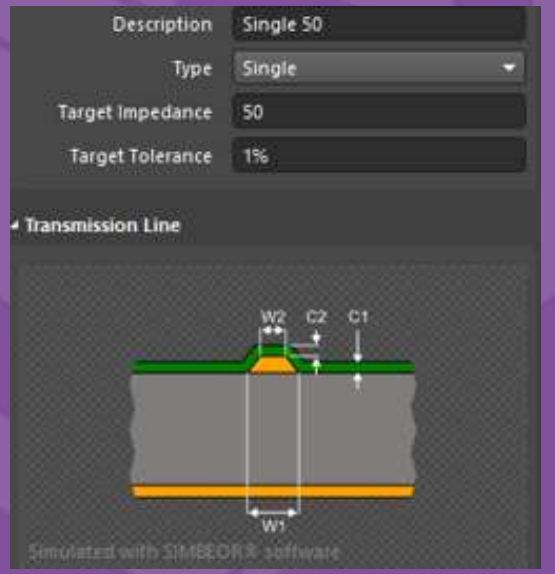


- Copper Loss (R)
- Dielectric Loss (G)
- Inductance (L)
- Capacitance (C)
-



Indipendent of lenght

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$



Losses

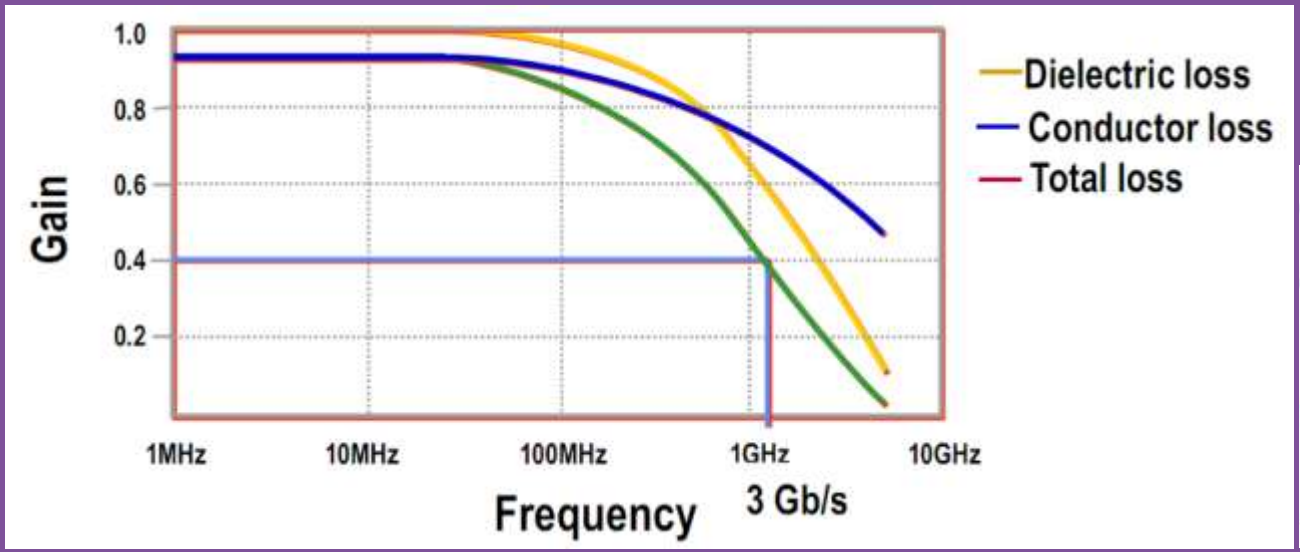
- Resistive loss
- Dielectric loss
- Radiated loss

Indipendent of lenght

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Indipendent of Frequency

$$Z_0 = \sqrt{\frac{L}{C}}$$



Frequency	FR4			4350		
	Copper Loss	Dielectric Loss	Total Loss	Copper Loss	Dielectric Loss	Total Loss
10 MHz	0.005	0.001	0.006	0.005	0.000	0.005
100 MHz	0.019	0.012	0.031	0.019	0.002	0.021
1 GHz	0.090	0.123	0.213	0.090	0.017	0.107
10 GHz	0.330	1.227	1.557	0.330	0.173	0.503

FR4 dielectric loss exceeds copper loss at 1 GHz

Losses - Conductor DC resistance

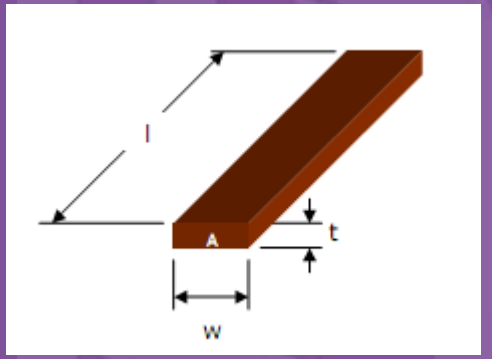
- Resistive losses
  - **Conductor DC resistance**
    - Geometry driven
    - Length dependent

DC Resistance

$$R_{DC} = \rho \frac{l}{tw} = \rho \frac{l}{A}$$

$$R_{DC} = 0.679\ \mu\Omega - in \frac{12\ in}{(0.0014\ in)(0.010\ in)} = 0.6\Omega$$

$$R_{DC} = 0.679\ \mu\Omega - in \frac{12\ in}{(0.0007\ in)(0.005\ in)} = 2.3\Omega$$



Resistive Loss – Skin depth

- Resistive losses
  - Conductor DC resistance
  - **Skin depth**
    - 2 µm @ 1 GHz
    - Effective conductor area is decreased!
    - **Increased resistive loss !**

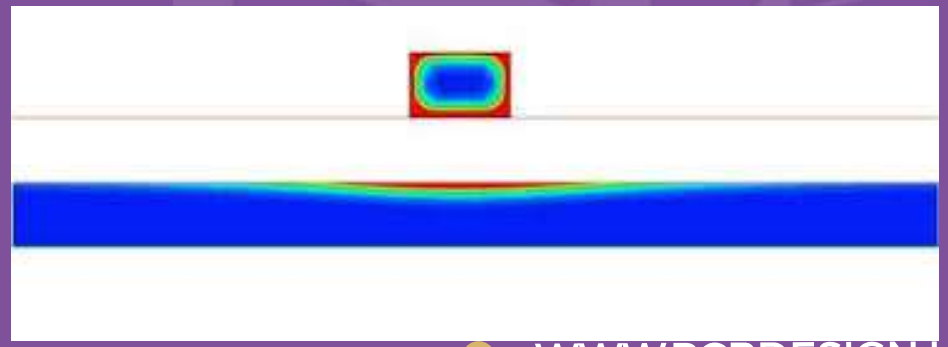
    - **1 oz (35 µm) , 1/2, 1/3 oz behaves similar**
    - **No cross coupling with common ground**

Skin Depth

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}}$$

$$\delta = \sqrt{\frac{0.0172\ \mu\Omega m}{\pi (10\,GHz)\left(4\pi x10^{-7}\ \frac{\Omega s}{m}\right)}} = 660\ nm = 0.03\ mils$$

$$\delta = \sqrt{\frac{0.0172\ \mu\Omega m}{\pi (10\,MHz)\left(4\pi x10^{-7}\ \frac{\Omega s}{m}\right)}} = 21\ \mu m = 0.8 mils$$

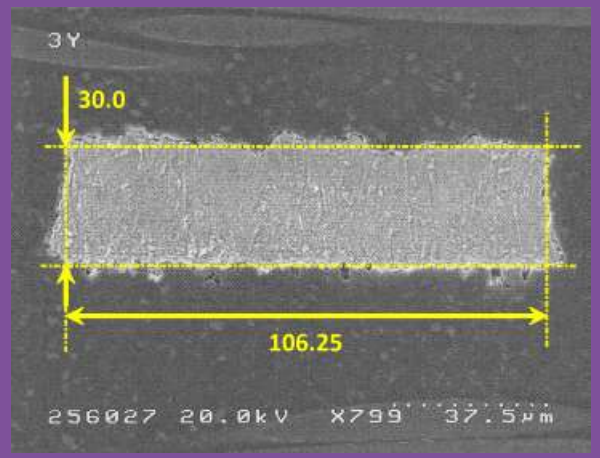


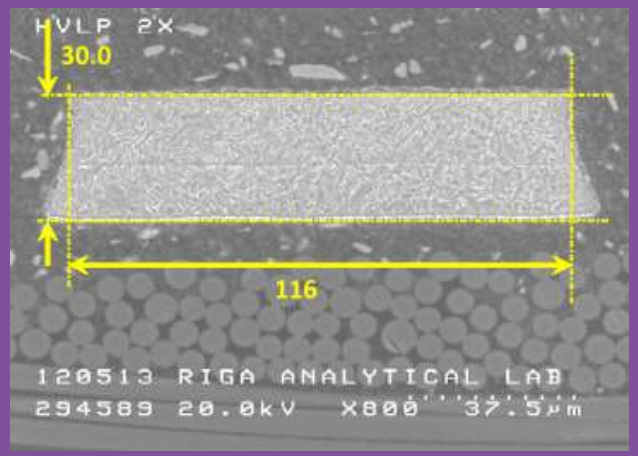
Resistive Loss – Surface roughness

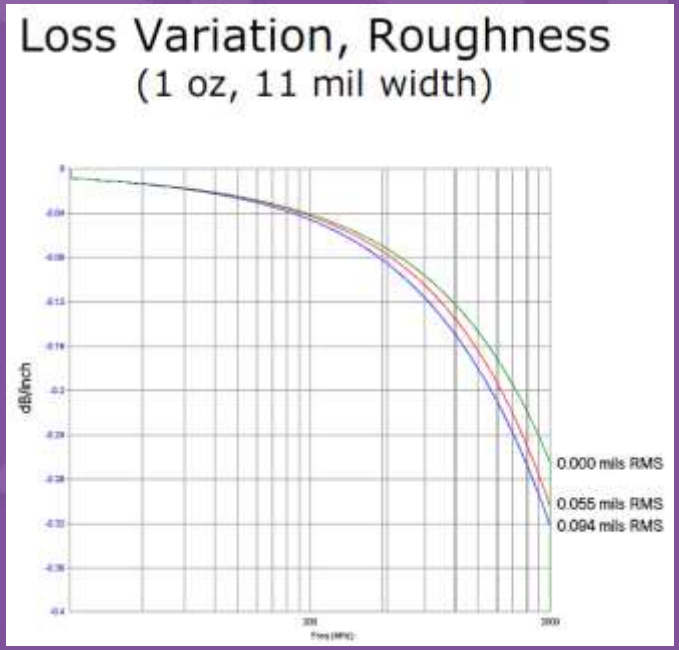
- Resistive losses
  - Conductor DC resistance
  - Skin depth
  - **Surface roughness**
    - **Above 1 GHz surface roughness increases signal length (skin depth)**

15" Transmission Line on mid-range material: ER=3.3, tanD=0.010

	PCIe® 3.0 - 4 GHz	PCIe® 4.0 - 8 GHz	PCIe® 5.0 - 16 GHz
Standard Foil (7-14um)	-6.9 dB	-12.3 dB	-21.8 dB
VLP (1-3um)	-6.4 dB +7%	-11.2 dB +9%	-19.9 dB +9%
HVLP (<1um)	-6.1 dB +12%	-10.6 dB +14%	-18.8 dB +14%







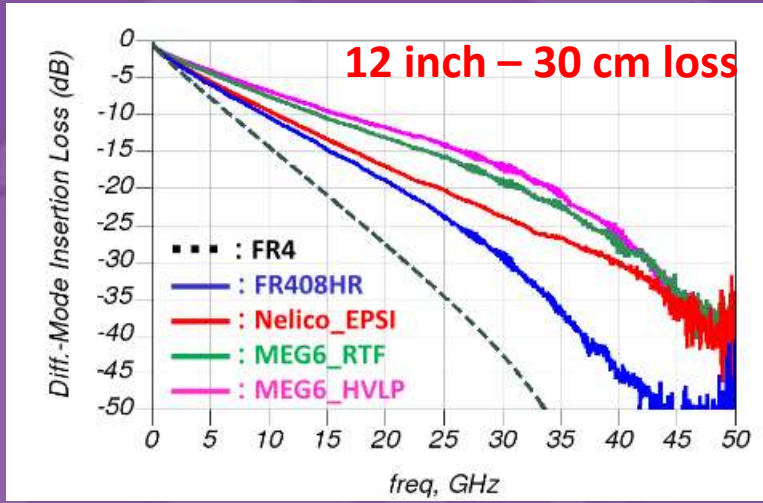
Dielectric loss

- Dielectric loss (G)
  - Dielectric loss exceeds resistive loss around 3 Gbit/s

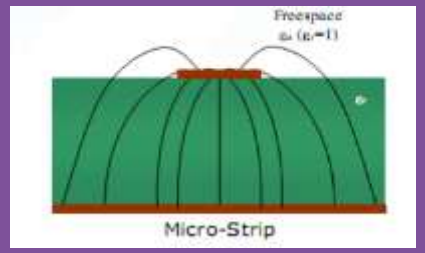
$$2.3\,(f)\tan(\theta)\sqrt{e_r}$$

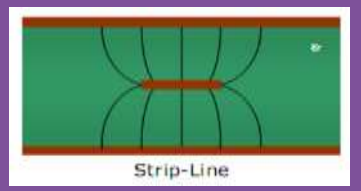
  - Material selection

Dk, Permittivity	A. @ 2 GHz B. @ 5 GHz C. @ 10 GHz	3.45
Df, Loss Tangent	A. @ 2 GHz B. @ 5 GHz C. @ 10 GHz	0.0031



  - Layer selection
    - **(Surface) microstrip losses are lower**



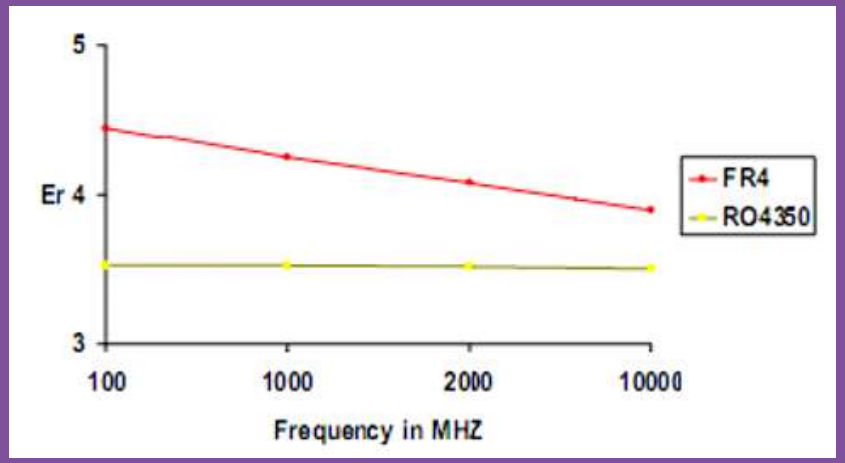


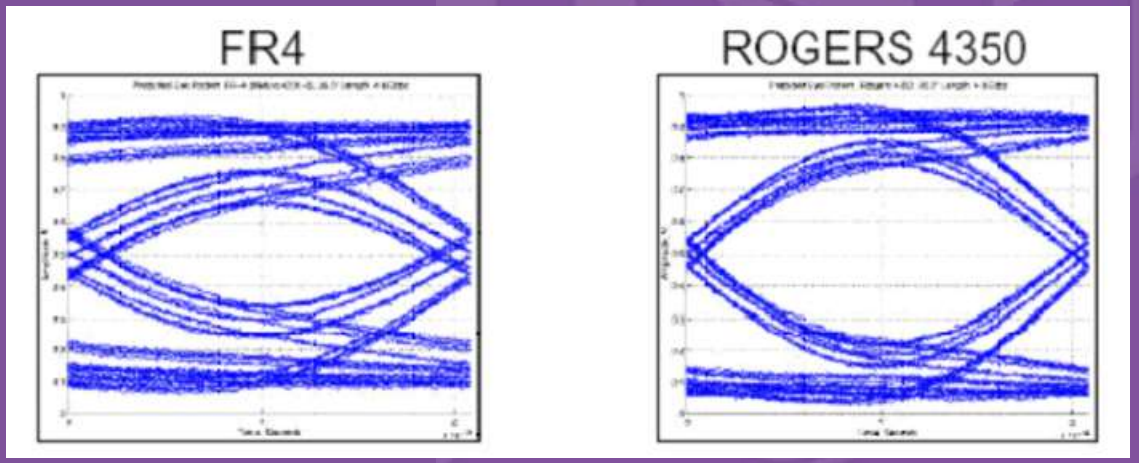
Loss frequency dependence

- Standard FR4 materials are not specified for high frequency operations. (Er is only defined at 1 Mhz)

- Dielectric constant is heavily frequency dependent

  →Signal dispersion





Practical summary

Use wider traces

- (+) Improves skin effect loss
- (+) No increase in material cost
- (-) Uses more routing area
- (-) Increases PCB thickness with fixed impedance

Use “High-speed” material

- (+) Lower Er → lowers dielectric loss
- (+) Lower loss tangent → lowers dielectric loss

Use “smooth” copper

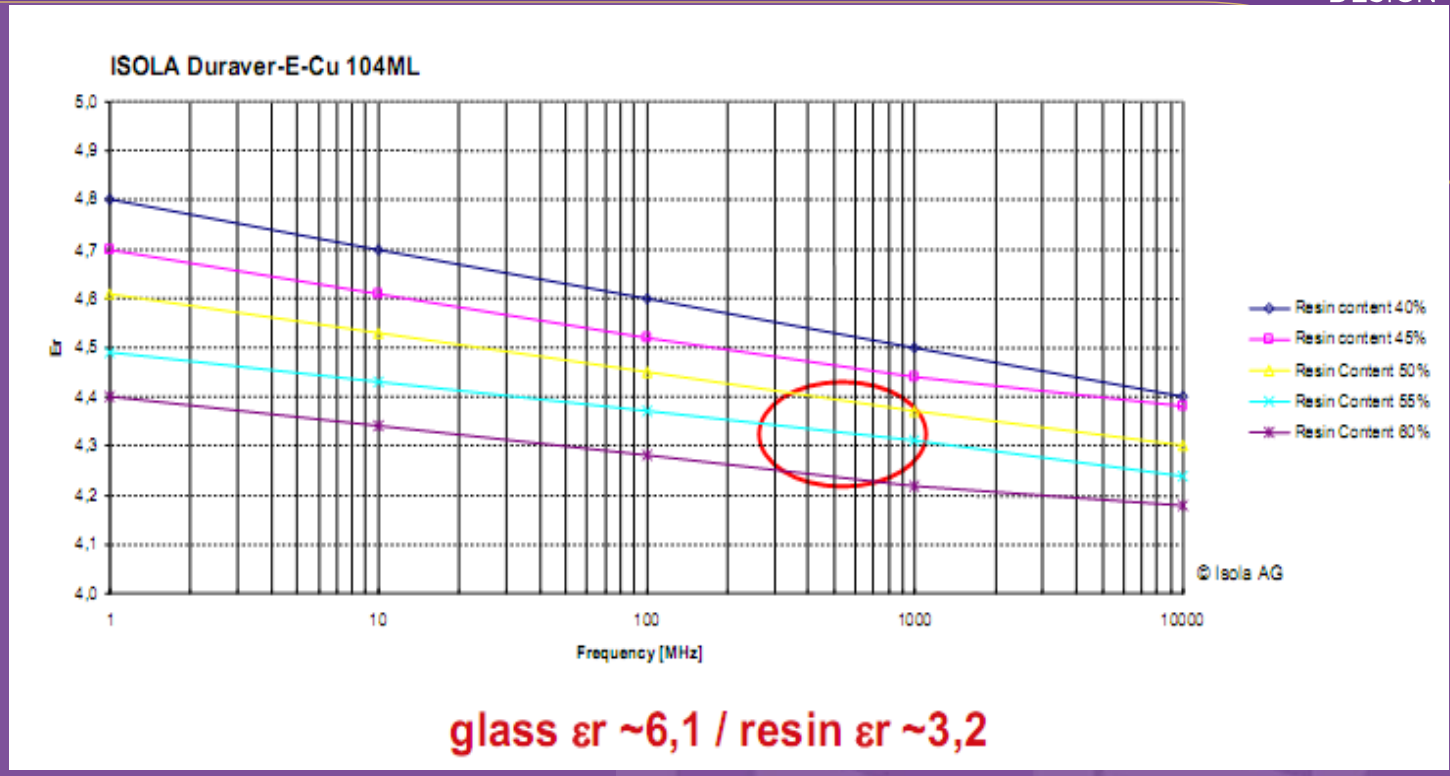
- (+) Lower dielectric loss
- (-) Caution! Peel strength is reduced

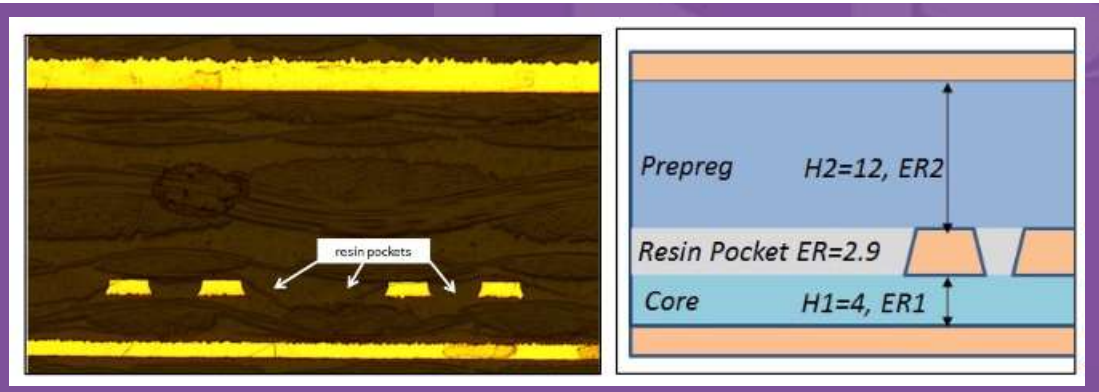
Effects of resin/glass content

Hard to predict impedance and loss

- Prepreg thickness dependent
- Temperature dependent
- Resin content changes during press

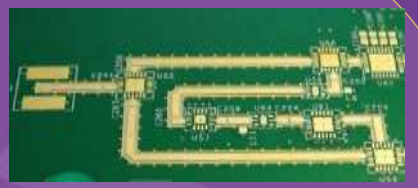
Zig-zag routing

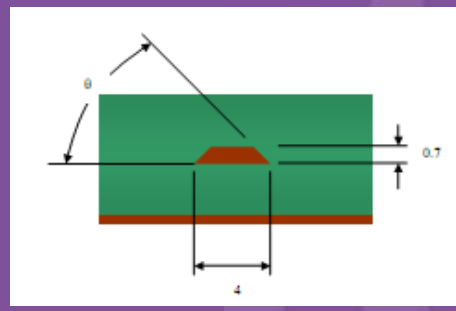




Etching / Thermal effects

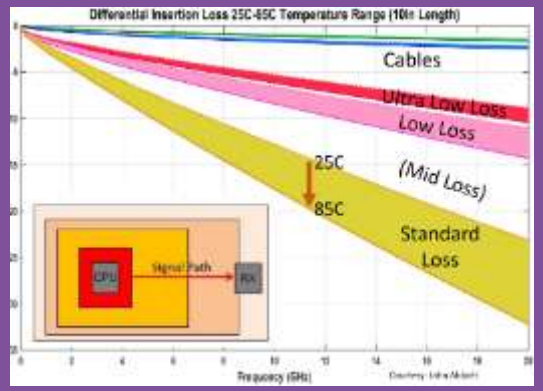
- **Outer layer anodization CU (+25-35um)**
- **Silkscreen / soldermask / coating effects**
- Etching (angle) significantly affects final impedance
  - Hard to maintain if unequal copper balance on a layer.





θ	L(nH/in)	C(pF/in)	Z_o (Ω)
90	8.5	3.4	50.0
79	8.6	3.3	50.7
72	8.6	3.3	51.0
60	8.7	3.3	51.5
45	8.8	3.2	52.2

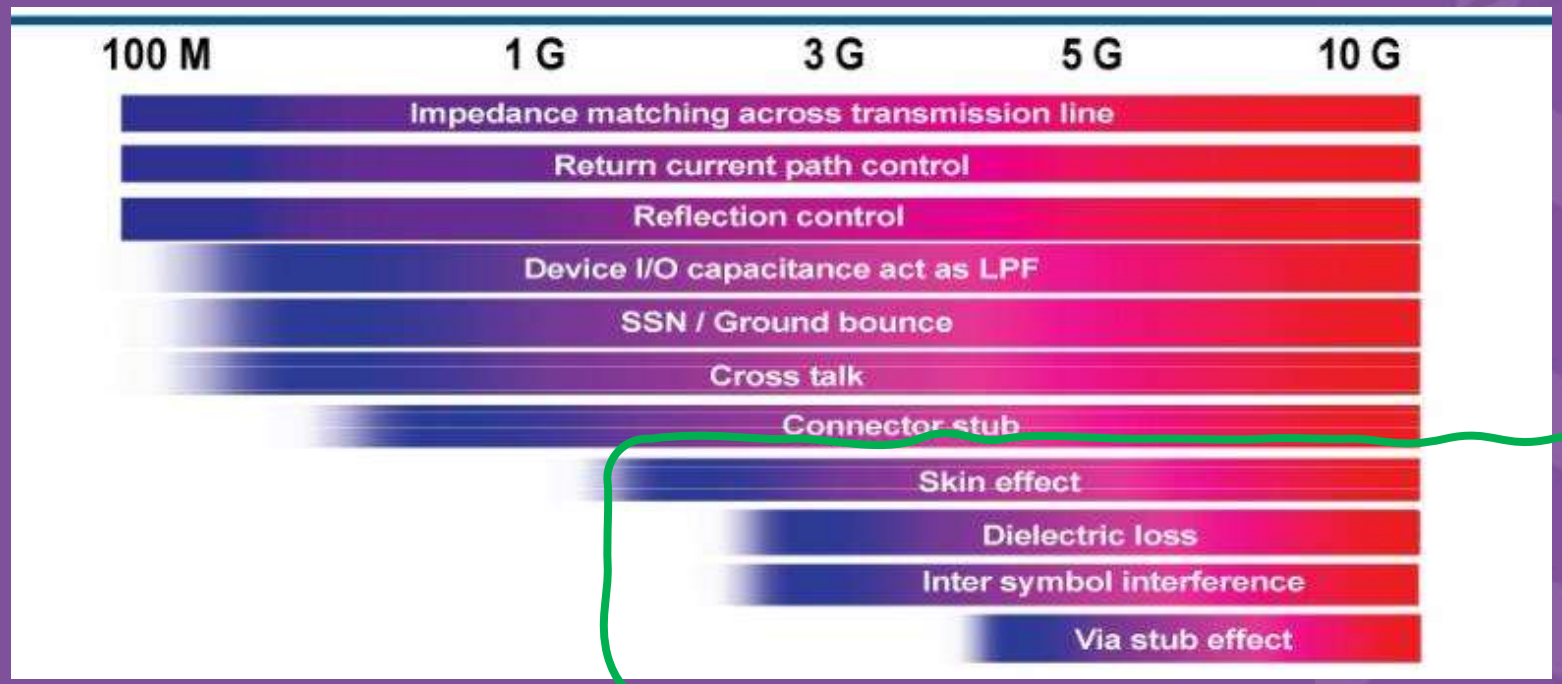
- Temperature rise increases loss



Nominal Loss (dB/inch at 4 GHz)	Microstrip Worst Case 75°C dB/inch (percentage increase)	Stripline Worst Case 75°C dB/inch (percentage increase)
0.40	0.50 (25%)	0.48 (19%)
0.44	0.54 (23%)	0.52 (17%)
0.5	0.60 (20%)	0.58 (15%)
0.6	0.70 (17%)	0.68 (13%)
0.7	0.93 (32%)	0.90 (29%)
0.8	1.03 (28%)	1.00 (25%)

Note: *Decibels per inch (dB/inch) is measured at 4 GHz.*

High speed design & layout

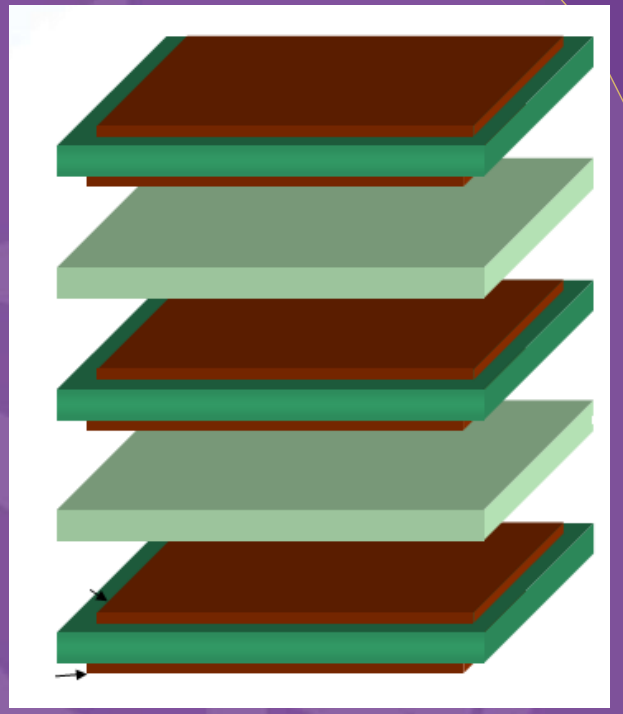


J.Zerbe / B. Nikolic

Optimal stackup planning

Stack up planning - basics

- Even number of layers
- Symmetrical structure prevent deformation
- Same thickness on both sides of the core

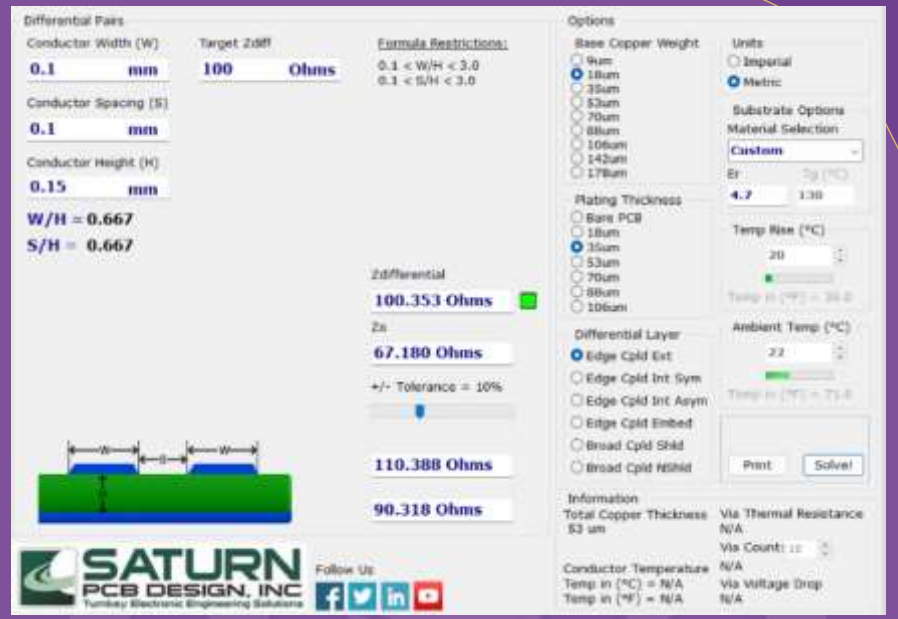


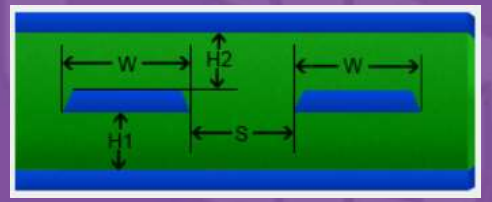
Steps:

- Determine technology (press cycles)
- Determine number of signal + power layers
- Assign ground layers
- Evaluate PCB thickness with “typical” impedances
- Adjust final thickness in the middle of the PCB

Stack up planning – Signal integrity effects

- Signal layers
  - Top/Bottom layer -Microstrip
    - 100 um for HDI- Er-3.4
    - 150 um for FR4
  - Inner layers (GSG) – Stripline
    - 150+150 um for HDI- Er-3.4
    - 250+250 um for FR4
  - Inner layers (GSSG) – Stripline
    - 100+300 um for HDI- Er-3.4 (85um line)
    - 200+400 um for FR4

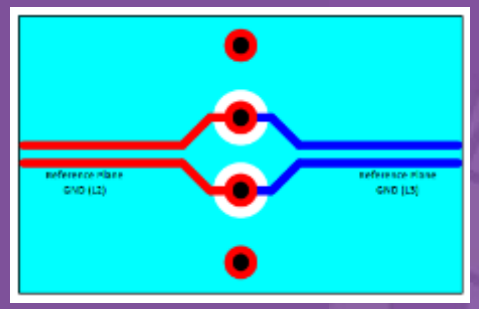


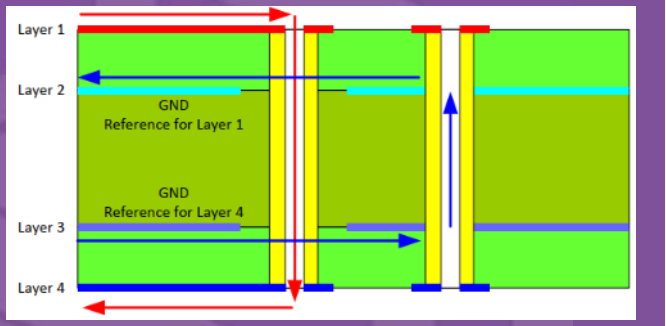


Stack up planning – Power layers

GND layers

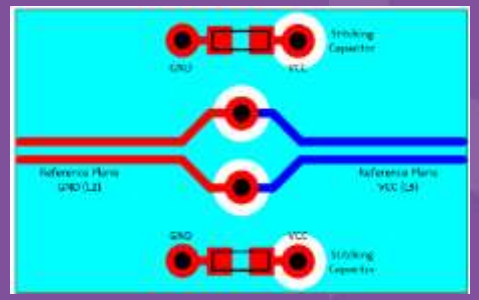
- Serve as reference layers for impedance control
- Stitching VIA between layers!
- EMI control
  - Shall be outward facing

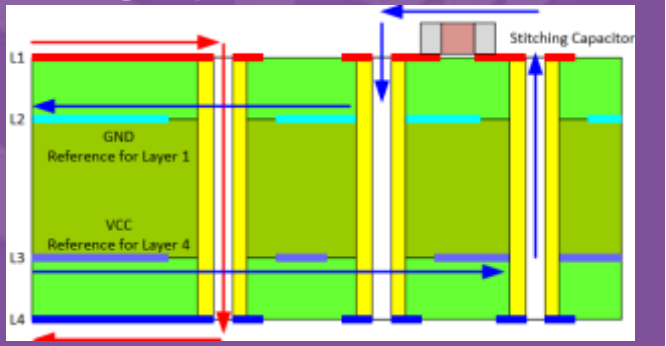




VCC layers

- Serve as plane capacitance (if big enough)
- Can act as impedance control reference (if big enough)





Stackup planning – Simple designs (4 layer)

- No impedance control planned
  - Reference layer is too far on microstrip (more 300 um)
    - GPS antenna on 2 layer PCB → Coplanar structure
    - Improper 4 layer stackup
  - Layer change effects
    - Propagation delay change
    - Impedance change
  - Signal is routed on power planes – no proper calculation
    - Copper pour is getting too close (unintentional coplanar)

copper - 1	18µm	½oz
Prepreg 7628	180µm	7mil
Prepreg 7628	180µm	7mil
copper - 2	35µm	1oz
Core	**710µm**	**27.95mil**
copper - 3	35µm	1oz
Prepreg 7628	180µm	7mil
Prepreg 7628	180µm	7mil
copper - 4	18µm	½oz

Stackup planning – Simple designs (6 layer)

- "The 6 layer problem"
  - Signal on layer 3
    - Too close to Signal on L4
    - Too far from reference on L
  - We would like to move Si
    - We shall maintain total thi
    - Not possible due to prepeg
  - Add 0 layer core in middle

8 Layer STD Build 1.55mm 0.062"		
copper - 1	18µm	½oz
Prepreg 2125	100µm	4mil
Prepreg 2125	100µm	4mil
copper - 2	35µm	1oz
Core	200µm	4mil
copper - 3	35µm	1oz
Prepreg 2125	100µm	4mil
Prepreg 2125	100µm	4mil
copper - 4	35µm	1oz
Core	200µm	4mil
copper - 5	35µm	1oz
Prepreg 2125	100µm	4mil
Prepreg 2125	100µm	4mil
copper - 6	35µm	1oz
Core	200µm	4mil
copper - 7	35µm	1oz
Prepreg 2125	100µm	4mil
Prepreg 2125	100µm	4mil
copper - 8	18µm	½oz

GND

SIG 1

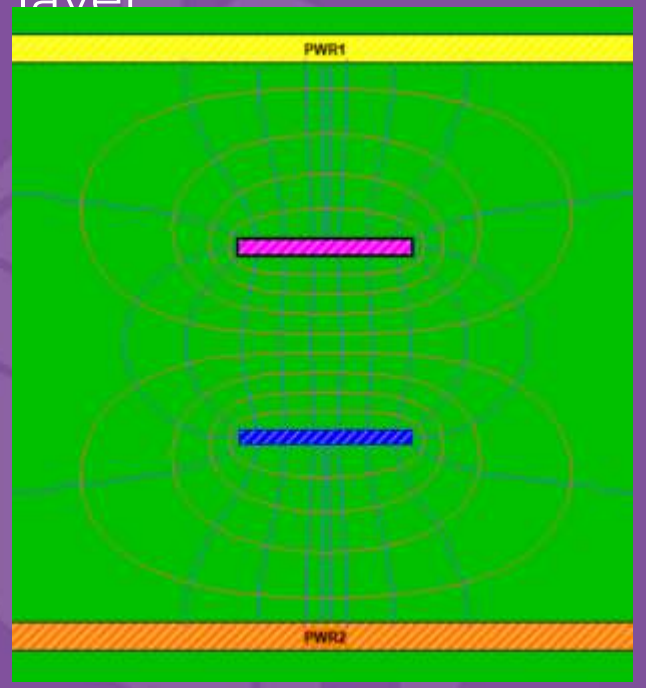
SIG 2

PWR

6 Layer STD Build 1.55mm 0.062"		
copper - 1	18µm	½oz
Prepreg 2125	100µm	4mil
Prepreg 2125	100µm	4mil
copper - 2	35µm	1oz
Core	360µm	14.2mil
copper - 3	35µm	1oz
Prepreg 7628	180µm	7mil
Prepreg 7628	180µm	7mil
copper - 4	35µm	1oz
Core	360µm	14.2mil
copper - 5	35µm	1oz
Prepreg 2125	100µm	4mil
Prepreg 2125	100µm	4mil
copper - 6	18µm	½oz

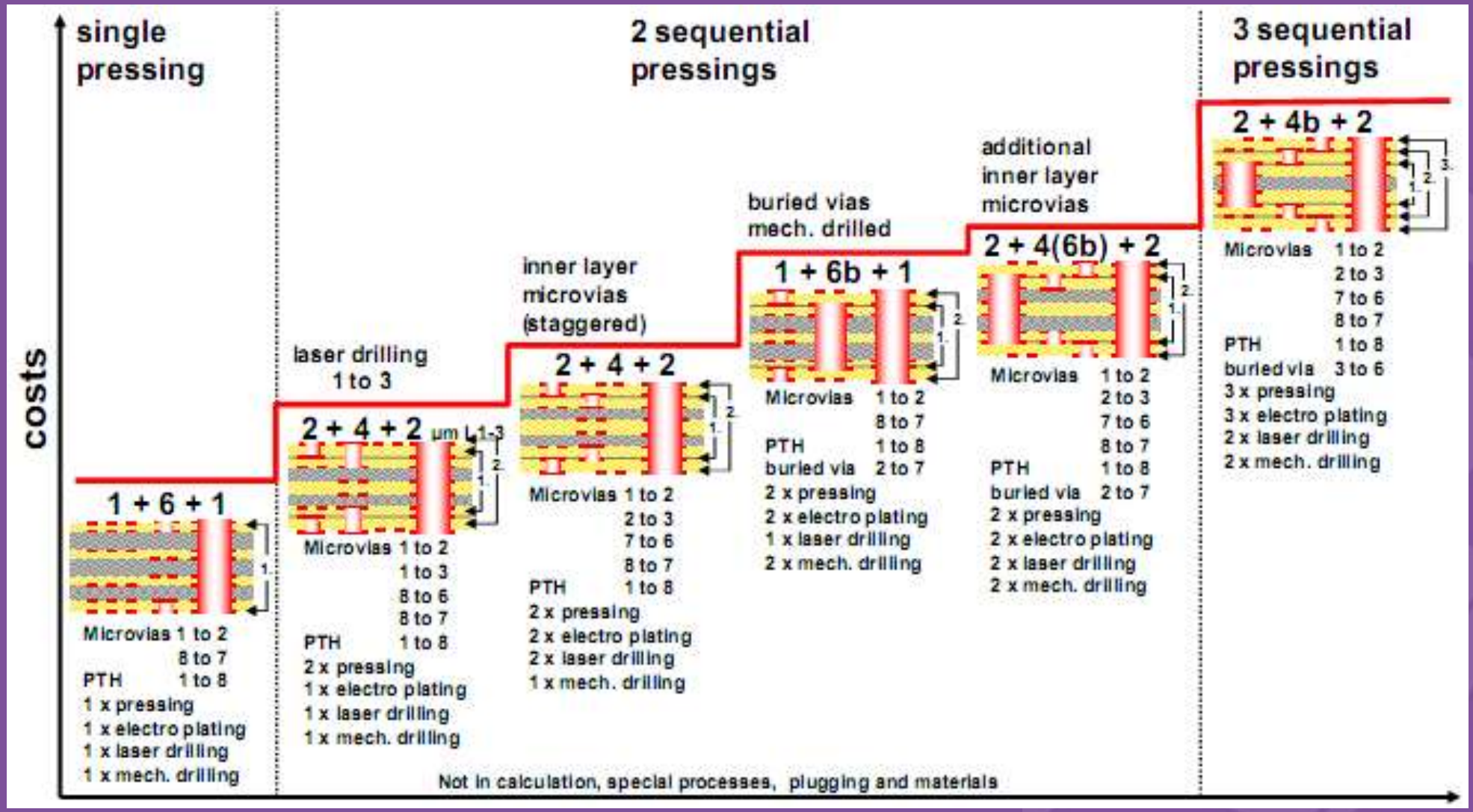
Stackup planning – More complex designs

- GSSG layer planning
  - Cheaper solution
  - Stripline reference should be further than adjacent signal layer
  - Horizontal / Vertical rooting



- GSG layer structure – 16+ layers
  - “Clean” design
  - Reference layer is too close on stripline
    - This would result two thick PCB or too think wiring
  - Hard to maintain PCB thickness
    - Low Er material is required
  - Class 3 production „problem” above 16 layers
    - VIA Drill size vs. annual ring vs aspect ratio
  - Top part of the PCB is hard to use efficiently

Microvia startegy – Cost factor

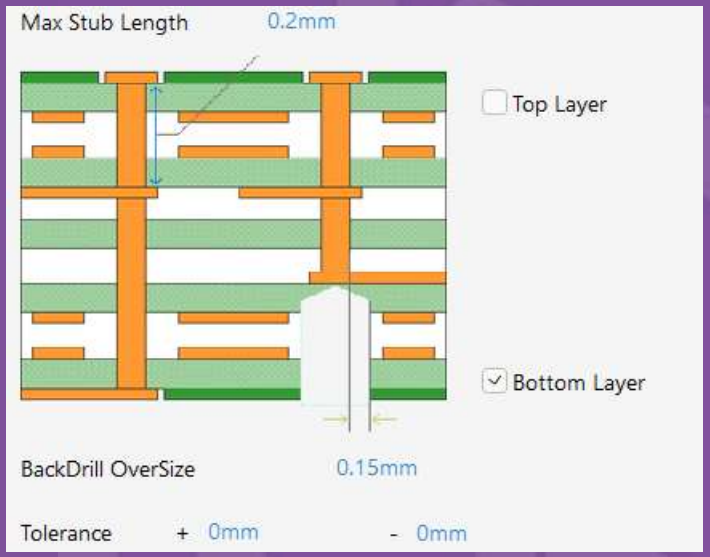


Source: Wurth Electronic

Minimizing the time for EQ/ TQ process

Proper documentation

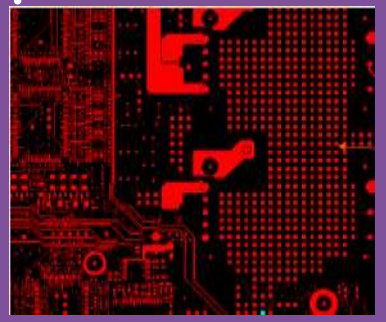
- Proper „self describing” manufacturing notes
  - Impedance requirements
    - Do not be too strict.
  - Drill/VIA information
    - Burried/ Blind VIA
    - Backdrill
      - Oversize
      - Depth tolerance
    - VIA tenting
      - Solder mask opening
  - VIA filling – CAP’ ing(IPC 4761 VII)

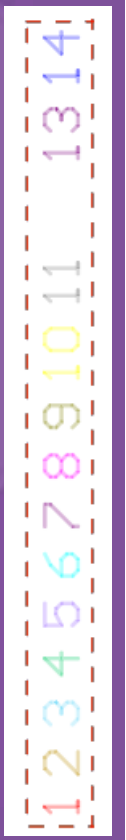


Proper documentation 2.

- Stackup adjustments and approval
  - Plan /**buy** manufacturer & (exact) material type in advance
  - Approach 1: Ask stackup/impedance and do design accordingly
  - Approach 2: Allow PCB manufacturer „slight” adjustments
    - Er adjustments (resin content/ material type) can be easily adjusted
    - Prepreg/core change - harder to compensate.
    - Check loss tangent too !

- Send separate impedance calculations
- Add layer marker on each gerber file.
- Thieving effects signal integrity.
  - Allow only on panel
- Unused PAD removal





Post layout impedance adjustments

- Use separate D-Code/ width

Differential Pairs

Conductor Width (W)
0.1 mm

Conductor Spacing (S)
0.1 mm

Conductor Height (H)
0.15 mm

W/H = 0.667
S/H = 0.667

Target Zdiff
100 Ohms

Formula Restrictions:
0.1 < W/H < 3.0
0.1 < S/H < 3.0

Differential Pairs

Conductor Width (W)
0.075 mm

Conductor Spacing (S)
0.125 mm

Conductor Height (H)
0.1 mm

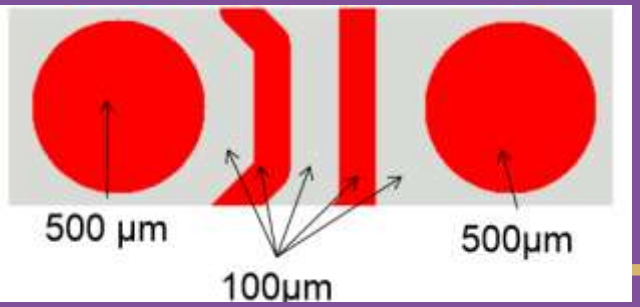
W/H = 0.750
S/H = 1.250

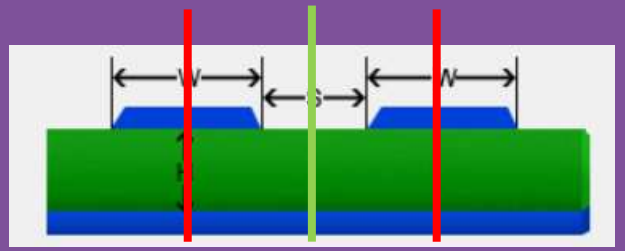
Target Zdiff
100 Ohms

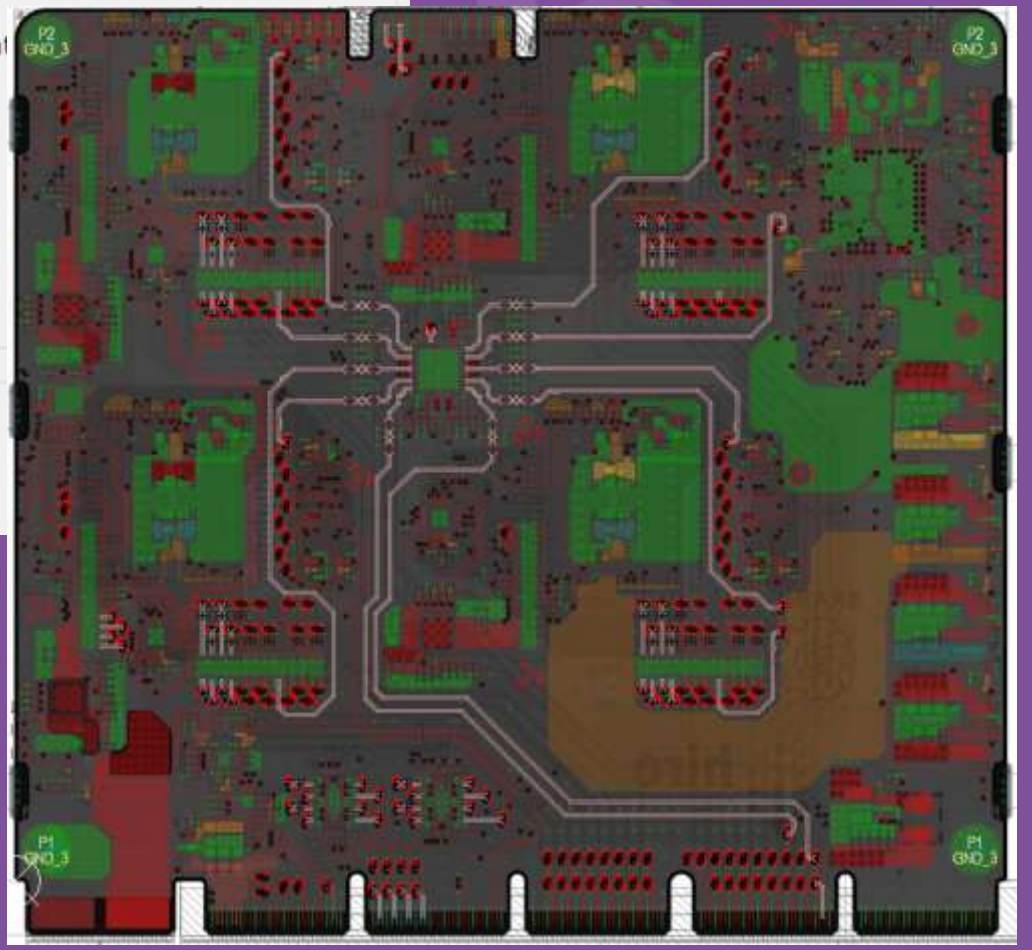
Options

Base Copper Weight
- 9um
- 18um
- 35um
- 53um
- 70um
- 88um
- 106um
- 142um
- 178um

Plating Thickness
- Bare PCB
- 18um
- 35um
- 53um

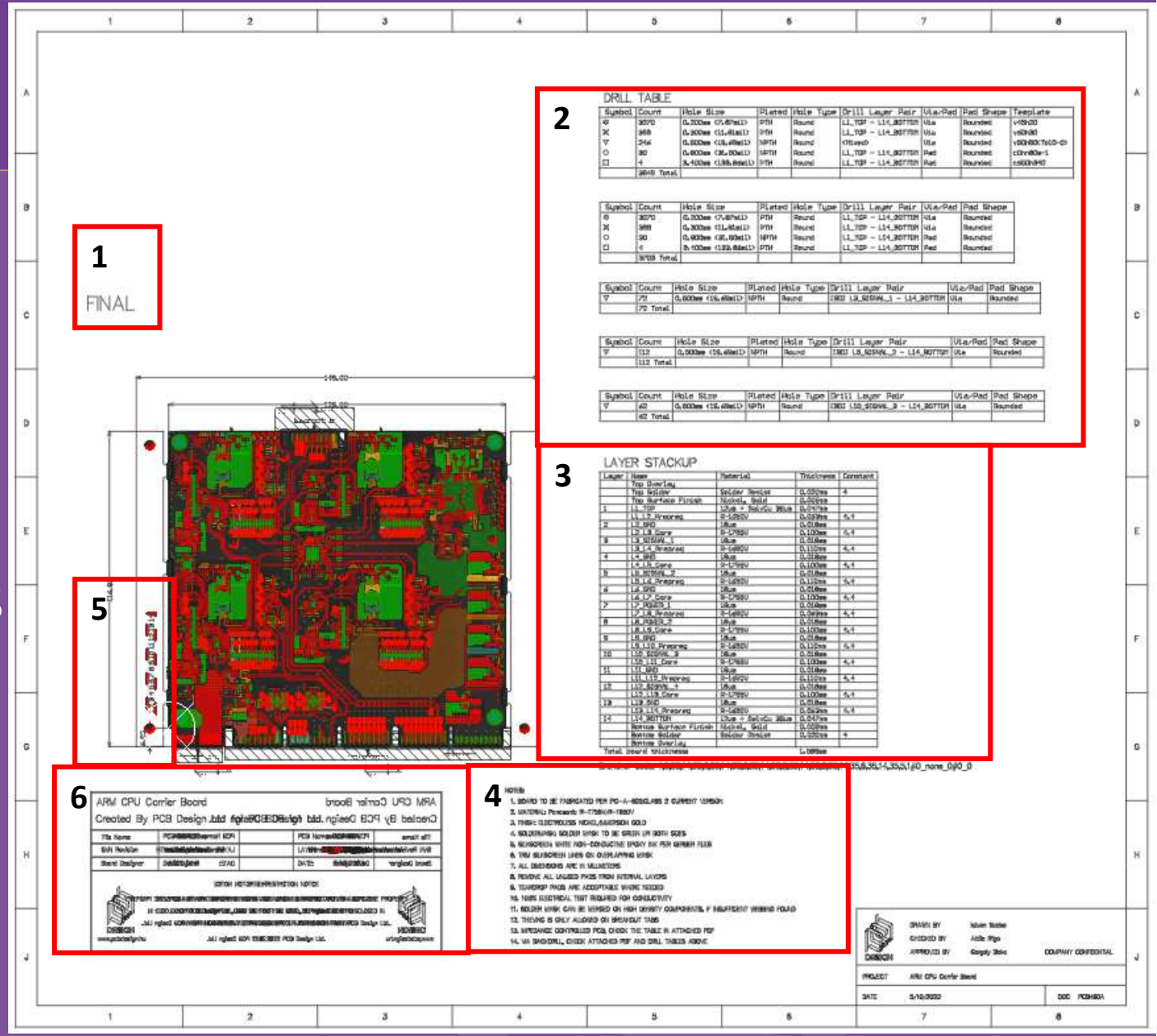






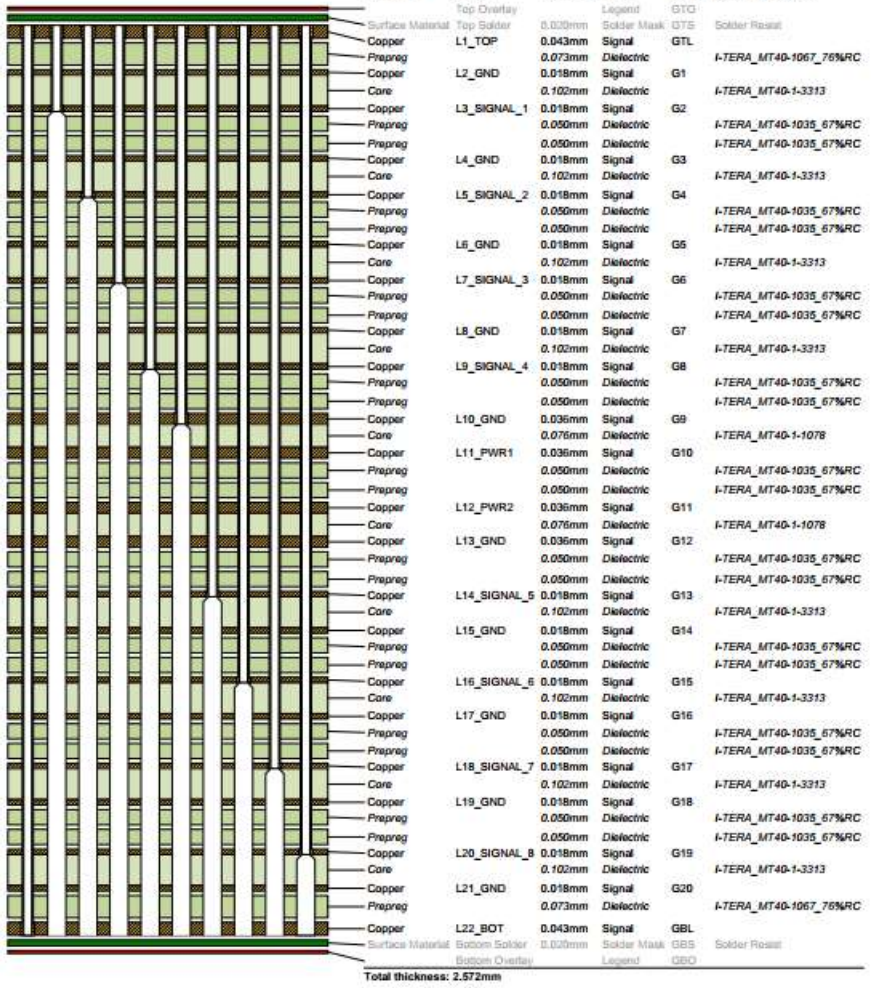
Practical example

- 1 – Version control
- 2 – Drill table
- 3 – Stackup/impedance
- table
- 4 – Manufacturing notes
- 5 – Layer marking
- 6 – Title box



Stackup / Impedance / Notes

LAYER STACKUP



Material	Layer	Thickness	Type	Gerber	Dielectric Material
	Top Overlay		Legend	GTO	
Surface Material	Top Solder	0.020mm	Solder Mask	GTS	Solder Resist
Copper	L1_TOP	0.043mm	Signal	GTL	
Prepreg		0.073mm	Dielectric		I-TERA_MT40-1067_76%RC
Copper	L2_GND	0.018mm	Signal	G1	
Core		0.102mm	Dielectric		I-TERA_MT40-1-3313
Copper	L3_SIGNAL_1	0.018mm	Signal	G2	
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Copper	L4_GND	0.018mm	Signal	G3	
Core		0.102mm	Dielectric		I-TERA_MT40-1-3313
Copper	L5_SIGNAL_2	0.018mm	Signal	G4	
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Copper	L6_GND	0.018mm	Signal	G5	
Core		0.102mm	Dielectric		I-TERA_MT40-1-3313
Copper	L7_SIGNAL_3	0.018mm	Signal	G6	
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Copper	L8_GND	0.018mm	Signal	G7	
Core		0.102mm	Dielectric		I-TERA_MT40-1-3313
Copper	L9_SIGNAL_4	0.018mm	Signal	G8	
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Copper	L10_GND	0.036mm	Signal	G9	
Core		0.076mm	Dielectric		I-TERA_MT40-1-1078
Copper	L11_PWR1	0.036mm	Signal	G10	
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Copper	L12_PWR2	0.036mm	Signal	G11	
Core		0.076mm	Dielectric		I-TERA_MT40-1-1078
Copper	L13_GND	0.036mm	Signal	G12	
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Copper	L14_SIGNAL_5	0.018mm	Signal	G13	
Core		0.102mm	Dielectric		I-TERA_MT40-1-3313
Copper	L15_GND	0.018mm	Signal	G14	
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Copper	L16_SIGNAL_6	0.018mm	Signal	G15	
Core		0.102mm	Dielectric		I-TERA_MT40-1-3313
Copper	L17_GND	0.018mm	Signal	G16	
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Copper	L18_SIGNAL_7	0.018mm	Signal	G17	
Core		0.102mm	Dielectric		I-TERA_MT40-1-3313
Copper	L19_GND	0.018mm	Signal	G18	
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Prepreg		0.050mm	Dielectric		I-TERA_MT40-1035_67%RC
Copper	L20_SIGNAL_8	0.018mm	Signal	G19	
Core		0.102mm	Dielectric		I-TERA_MT40-1-3313
Copper	L21_GND	0.018mm	Signal	G20	
Prepreg		0.073mm	Dielectric		I-TERA_MT40-1067_76%RC
Copper	L22_BOT	0.043mm	Signal	GBL	
Surface Material	Bottom Solder	0.020mm	Solder Mask	GBS	Solder Resist
	Bottom Overlay		Legend	GBO	

Total thickness: 2.572mm

IMPEDANCE TABLE

Target Impedance	Trace layer	Trace Width	Gap	Reference layers
100	L1_TOP	0.089mm	0.127mm	L2_GND
90	L1_TOP	0.117mm	0.110mm	L2_GND
50	L1_TOP	0.127mm		L2_GND
100	L3_SIGNAL_1	0.089mm	0.114mm	L2_GND,L4_GND
100	L3_SIGNAL_1	0.075mm	0.100mm	L2_GND,L4_GND
50	L3_SIGNAL_1	0.107mm		L2_GND,L4_GND
100	L5_SIGNAL_2	0.089mm	0.114mm	L4_GND,L6_GND
100	L5_SIGNAL_2	0.075mm	0.100mm	L4_GND,L6_GND
90	L5_SIGNAL_2	0.090mm	0.100mm	L4_GND,L6_GND
90	L5_SIGNAL_2	0.082mm	0.085mm	L4_GND,L6_GND
50	L5_SIGNAL_2	0.107mm		L4_GND,L6_GND
39	L5_SIGNAL_2	0.146mm		L4_GND,L6_GND
100	L7_SIGNAL_3	0.089mm	0.114mm	L6_GND,L8_GND
100	L7_SIGNAL_3	0.075mm	0.100mm	L6_GND,L8_GND
66	L7_SIGNAL_3	0.177mm	0.120mm	L6_GND,L8_GND
50	L7_SIGNAL_3	0.107mm		L6_GND,L8_GND
39	L7_SIGNAL_3	0.146mm		L6_GND,L8_GND
100	L9_SIGNAL_4	0.089mm	0.114mm	L8_GND,L10_GND
100	L9_SIGNAL_4	0.075mm	0.100mm	L8_GND,L10_GND
50	L9_SIGNAL_4	0.107mm		L8_GND,L10_GND
100	L14_SIGNAL_5	0.089mm	0.114mm	L13_GND,L15_GND
100	L14_SIGNAL_5	0.075mm	0.100mm	L13_GND,L15_GND
90	L14_SIGNAL_5	0.090mm	0.100mm	L13_GND,L15_GND
90	L14_SIGNAL_5	0.082mm	0.085mm	L13_GND,L15_GND
66	L14_SIGNAL_5	0.177mm	0.120mm	L13_GND,L15_GND
50	L14_SIGNAL_5	0.107mm		L13_GND,L15_GND
39	L14_SIGNAL_5	0.146mm		L13_GND,L15_GND
100	L16_SIGNAL_6	0.089mm	0.114mm	L15_GND,L17_GND
100	L16_SIGNAL_6	0.075mm	0.100mm	L15_GND,L17_GND
90	L16_SIGNAL_6	0.090mm	0.100mm	L15_GND,L17_GND
90	L16_SIGNAL_6	0.082mm	0.085mm	L15_GND,L17_GND
66	L16_SIGNAL_6	0.177mm	0.120mm	L15_GND,L17_GND
50	L16_SIGNAL_6	0.107mm		L15_GND,L17_GND
39	L16_SIGNAL_6	0.146mm		L15_GND,L17_GND
100	L18_SIGNAL_7	0.089mm	0.114mm	L17_GND,L19_GND
100	L18_SIGNAL_7	0.075mm	0.100mm	L17_GND,L19_GND
90	L18_SIGNAL_7	0.090mm	0.100mm	L17_GND,L19_GND
90	L18_SIGNAL_7	0.082mm	0.085mm	L17_GND,L19_GND
66	L18_SIGNAL_7	0.177mm	0.120mm	L17_GND,L19_GND
50	L18_SIGNAL_7	0.107mm		L17_GND,L19_GND
39	L18_SIGNAL_7	0.146mm		L17_GND,L19_GND
100	L20_SIGNAL_8	0.089mm	0.114mm	L19_GND,L21_GND
100	L20_SIGNAL_8	0.075mm	0.100mm	L19_GND,L21_GND
90	L20_SIGNAL_8	0.090mm	0.100mm	L19_GND,L21_GND
90	L20_SIGNAL_8	0.082mm	0.085mm	L19_GND,L21_GND
66	L20_SIGNAL_8	0.177mm	0.120mm	L19_GND,L21_GND
50	L20_SIGNAL_8	0.107mm		L19_GND,L21_GND
39	L20_SIGNAL_8	0.146mm		L19_GND,L21_GND
100	L22_BOT	0.089mm	0.127mm	L21_GND
90	L22_BOT	0.117mm	0.110mm	L21_GND
50	L22_BOT	0.127mm		L21_GND

NOTES

TECHNICAL PARAMETERS	
Material	I-TERA MT40
Layer count	22 layers
Via Size	0.2/0.5mm
Via tenting	Top-Bottom Tenting
Via filling	TYPE-VII VIA FILLING
Buried Via	no
Blind/Micro via	no
Backdrill	yes
Minimum track width/clearance	0.075mm/0.085mm
Impedance	Impendance controlled
Surface finish	ENIG
Solder mask	LPI Green x2
Silkscreen	White
IPC Class	Class III
IPC Class Waiver	VIA Waiver
STENCIL	
Required	no
MECHANICAL PARAMETERS	
Panelisation	In Gerber
Panel Dimension	430x323.4mm
PCB Dimension	458x298.4mm
SPECIAL REMARKS	
1	PTH tolerance: check notes on gerber
2	N/A

Q & A

DESIGN

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